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**********************************************************
    1466 Tue Jun 17 10:46:17 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/THIRDPARTYLICENSE
NEX-1888 upstream
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      42 Tue Jun 17 10:46:17 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/THIRDPARTYLICENSE.descrip
NEX-1888 upstream
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   1 LSI Fusion-MPT MPI 2.0 / 2.5 Header Files
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   54260 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2.h
NEX-1888 upstream
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```
/*-
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 * DAMAGE.
 */

/*
 *          Name:  mpi2.h
 *         Title:  MPI Message independent structures and definitions
 *                 including System Interface Register Set and
 *                 scatter/gather formats.
 *  Creation Date:  June 21, 2006
 *
 *  mpi2.h Version:  02.00.33
 *  mpi2.h Version:  02.00.13
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-04-07  02.00.01  Bumped MPI2_HEADER_VERSION_UNIT.
 *  06-26-07  02.00.02  Bumped MPI2_HEADER_VERSION_UNIT.
 *  08-31-07  02.00.03  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Moved ReplyPostHostIndex register to offset 0x6C of the
 *                      MPI2_SYSTEM_INTERFACE_REGS and modified the define for
 *                      MPI2_REPLY_POST_HOST_INDEX_OFFSET.
 *                      Added union of request descriptors.
 *                      Added union of reply descriptors.
 *  10-31-07  02.00.04  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added define for MPI2_VERSION_02_00.
 *                      Fixed the size of the FunctionDependent5 field in the
 *                      MPI2_DEFAULT_REPLY structure.
 *  12-18-07  02.00.05  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Removed the MPI-defined Fault Codes and extended the
 *                      product specific codes up to 0xEFFF.
 *                      Added a sixth key value for the WriteSequence register
 *                      and changed the flush value to 0x0.
 *                      Added message function codes for Diagnostic Buffer Post
 *                      and Diagnsotic Release.
 *                      New IOCStatus define: MPI2_IOCSTATUS_DIAGNOSTIC_RELEASED
 *                      Moved MPI2_VERSION_UNION from mpi2_ioc.h.
 *  02-29-08  02.00.06  Bumped MPI2_HEADER_VERSION_UNIT.
 *  03-03-08  02.00.07  Bumped MPI2_HEADER_VERSION_UNIT.
 *  05-21-08  02.00.08  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added #defines for marking a reply descriptor as unused.
 *  06-27-08  02.00.09  Bumped MPI2_HEADER_VERSION_UNIT.
 *  10-02-08  02.00.10  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Moved LUN field defines from mpi2_init.h.
 *  01-19-09  02.00.11  Bumped MPI2_HEADER_VERSION_UNIT.
 *  05-06-09  02.00.12  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      In all request and reply descriptors, replaced VF_ID
 *                      field with MSIxIndex field.
```

```
 85  *                     Removed DevHandle field from
 86  *                     MPI2_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR and made those
 87  *                     bytes reserved.
 88  *                     Added RAID Accelerator functionality.
 89  *  07-30-09  02.00.13 Bumped MPI2_HEADER_VERSION_UNIT.
 90  *  10-28-09  02.00.14 Bumped MPI2_HEADER_VERSION_UNIT.
 91  *                     Added MSI-x index mask and shift for Reply Post Host
 92  *                     Index register.
 93  *                     Added function code for Host Based Discovery Action.
 94  *  02-10-10  02.00.15 Bumped MPI2_HEADER_VERSION_UNIT.
 95  *                     Added define for MPI2_FUNCTION_PWR_MGMT_CONTROL.
 96  *                     Added defines for product-specific range of message
 97  *                     function codes, 0xF0 to 0xFF.
 98  *  05-12-10  02.00.16 Bumped MPI2_HEADER_VERSION_UNIT.
 99  *                     Added alternative defines for the SGE Direction bit.
100  *  08-11-10  02.00.17 Bumped MPI2_HEADER_VERSION_UNIT.
101  *  11-10-10  02.00.18 Bumped MPI2_HEADER_VERSION_UNIT.
102  *                     Added MPI2_IEEE_SGE_FLAGS_SYSTEMPLBCPI_ADDR define.
103  *  02-23-11  02.00.19 Bumped MPI2_HEADER_VERSION_UNIT.
104  *                     Added MPI2_FUNCTION_SEND_HOST_MESSAGE.
105  *  03-09-11  02.00.20 Bumped MPI2_HEADER_VERSION_UNIT.
106  *  05-25-11  02.00.21 Bumped MPI2_HEADER_VERSION_UNIT.
107  *  08-24-11  02.00.22 Bumped MPI2_HEADER_VERSION_UNIT.
108  *  11-18-11  02.00.23 Bumped MPI2_HEADER_VERSION_UNIT.
109  *                     Incorporating additions for MPI v2.5.
110  *  02-06-12  02.00.24 Bumped MPI2_HEADER_VERSION_UNIT.
111  *  03-29-12  02.00.25 Bumped MPI2_HEADER_VERSION_UNIT.
112  *                     Added Hard Reset delay timings.
113  *  07-10-12  02.00.26 Bumped MPI2_HEADER_VERSION_UNIT.
114  *  07-26-12  02.00.27 Bumped MPI2_HEADER_VERSION_UNIT.
115  *  11-27-12  02.00.28 Bumped MPI2_HEADER_VERSION_UNIT.
116  *  12-20-12  02.00.29 Bumped MPI2_HEADER_VERSION_UNIT.
117  *                     Added MPI25_SUP_REPLY_POST_HOST_INDEX_OFFSET.
118  *  04-09-13  02.00.30 Bumped MPI2_HEADER_VERSION_UNIT.
119  *  04-17-13  02.00.31 Bumped MPI2_HEADER_VERSION_UNIT.
120  *  08-19-13  02.00.32 Bumped MPI2_HEADER_VERSION_UNIT.
121  *  12-05-13  02.00.33 Bumped MPI2_HEADER_VERSION_UNIT.
122  *  --------------------------------------------------------------------------
123  */

125 #ifndef MPI2_H
126 #define MPI2_H


129 /*****************************************************************************
130 *
131 *        MPI Version Definitions
132 *
133 *****************************************************************************/

114 #define MPI2_VERSION_MAJOR                  (0x02)
115 #define MPI2_VERSION_MINOR                  (0x00)
135 #define MPI2_VERSION_MAJOR_MASK             (0xFF00)
136 #define MPI2_VERSION_MAJOR_SHIFT            (8)
137 #define MPI2_VERSION_MINOR_MASK             (0x00FF)
138 #define MPI2_VERSION_MINOR_SHIFT            (0)

140 /* major version for all MPI v2.x */
141 #define MPI2_VERSION_MAJOR                  (0x02)

143 /* minor version for MPI v2.0 compatible products */
144 #define MPI2_VERSION_MINOR                  (0x00)
145 #define MPI2_VERSION (((MPI2_VERSION_MAJOR << MPI2_VERSION_MAJOR_SHIFT) |   \
146                                     MPI2_VERSION_MINOR)

147 #define MPI2_VERSION_02_00                  (0x0200)
```



```
150 /* minor version for MPI v2.5 compatible products */
151 #define MPI25_VERSION_MINOR                 (0x05)
152 #define MPI25_VERSION ((MPI2_VERSION_MAJOR << MPI2_VERSION_MAJOR_SHIFT) |   \
153                                             MPI25_VERSION_MINOR)
154 #define MPI2_VERSION_02_05                  (0x0205)


157 /* Unit and Dev versioning for this MPI header set */
158 #define MPI2_HEADER_VERSION_UNIT            (0x21)
125 /* versioning for this MPI header set */
126 #define MPI2_HEADER_VERSION_UNIT            (0x0D)
159 #define MPI2_HEADER_VERSION_DEV             (0x00)
160 #define MPI2_HEADER_VERSION_UNIT_MASK       (0xFF00)
161 #define MPI2_HEADER_VERSION_UNIT_SHIFT      (8)
162 #define MPI2_HEADER_VERSION_DEV_MASK        (0x00FF)
163 #define MPI2_HEADER_VERSION_DEV_SHIFT       (0)
164 #define MPI2_HEADER_VERSION ((MPI2_HEADER_VERSION_UNIT << 8) | MPI2_HEADER_VERSI


167 /*****************************************************************************
168 *
169 *        IOC State Definitions
170 *
171 *****************************************************************************/

173 #define MPI2_IOC_STATE_RESET                (0x00000000)
174 #define MPI2_IOC_STATE_READY                (0x10000000)
175 #define MPI2_IOC_STATE_OPERATIONAL          (0x20000000)
176 #define MPI2_IOC_STATE_FAULT                (0x40000000)

178 #define MPI2_IOC_STATE_MASK                 (0xF0000000)
179 #define MPI2_IOC_STATE_SHIFT                (28)

181 /* Fault state range for prodcut specific codes */
182 #define MPI2_FAULT_PRODUCT_SPECIFIC_MIN                 (0x0000)
183 #define MPI2_FAULT_PRODUCT_SPECIFIC_MAX                 (0xEFFF)


186 /*****************************************************************************
187 *
188 *        System Interface Register Definitions
189 *
190 *****************************************************************************/

192 typedef volatile struct _MPI2_SYSTEM_INTERFACE_REGS
193 {
194     U32         Doorbell;                   /* 0x00 */
195     U32         WriteSequence;              /* 0x04 */
196     U32         HostDiagnostic;             /* 0x08 */
197     U32         Reserved1;                  /* 0x0C */
198     U32         DiagRWData;                 /* 0x10 */
199     U32         DiagRWAddressLow;           /* 0x14 */
200     U32         DiagRWAddressHigh;          /* 0x18 */
201     U32         Reserved2[5];               /* 0x1C */
202     U32         HostInterruptStatus;        /* 0x30 */
203     U32         HostInterruptMask;          /* 0x34 */
204     U32         DCRData;                    /* 0x38 */
205     U32         DCRAddress;                 /* 0x3C */
206     U32         Reserved3[2];               /* 0x40 */
207     U32         ReplyFreeHostIndex;         /* 0x48 */
208     U32         Reserved4[8];               /* 0x4C */
209     U32         ReplyPostHostIndex;         /* 0x6C */
210     U32         Reserved5;                  /* 0x70 */
211     U32         HCBSize;                    /* 0x74 */
```

```
212     U32         HCBAddressLow;              /* 0x78 */
213     U32         HCBAddressHigh;             /* 0x7C */
214     U32         Reserved6[16];              /* 0x80 */
215     U32         RequestDescriptorPostLow;   /* 0xC0 */
216     U32         RequestDescriptorPostHigh;  /* 0xC4 */
217     U32         Reserved7[14];              /* 0xC8 */
218 } MPI2_SYSTEM_INTERFACE_REGS, MPI2_POINTER PTR_MPI2_SYSTEM_INTERFACE_REGS,
219   Mpi2SystemInterfaceRegs_t, MPI2_POINTER pMpi2SystemInterfaceRegs_t;

221 /*
222  * Defines for working with the Doorbell register.
223  */
224 #define MPI2_DOORBELL_OFFSET                    (0x00000000)

226 /* IOC --> System values */
227 #define MPI2_DOORBELL_USED                      (0x08000000)
228 #define MPI2_DOORBELL_WHO_INIT_MASK             (0x07000000)
229 #define MPI2_DOORBELL_WHO_INIT_SHIFT            (24)
230 #define MPI2_DOORBELL_FAULT_CODE_MASK           (0x0000FFFF)
231 #define MPI2_DOORBELL_DATA_MASK                 (0x0000FFFF)

233 /* System --> IOC values */
234 #define MPI2_DOORBELL_FUNCTION_MASK             (0xFF000000)
235 #define MPI2_DOORBELL_FUNCTION_SHIFT            (24)
236 #define MPI2_DOORBELL_ADD_DWORDS_MASK           (0x00FF0000)
237 #define MPI2_DOORBELL_ADD_DWORDS_SHIFT          (16)


240 /*
241  * Defines for the WriteSequence register
242  */
243 #define MPI2_WRITE_SEQUENCE_OFFSET              (0x00000004)
244 #define MPI2_WRSEQ_KEY_VALUE_MASK               (0x0000000F)
245 #define MPI2_WRSEQ_FLUSH_KEY_VALUE              (0x0)
246 #define MPI2_WRSEQ_1ST_KEY_VALUE                (0xF)
247 #define MPI2_WRSEQ_2ND_KEY_VALUE                (0x4)
248 #define MPI2_WRSEQ_3RD_KEY_VALUE                (0xB)
249 #define MPI2_WRSEQ_4TH_KEY_VALUE                (0x2)
250 #define MPI2_WRSEQ_5TH_KEY_VALUE                (0x7)
251 #define MPI2_WRSEQ_6TH_KEY_VALUE                (0xD)

253 /*
254  * Defines for the HostDiagnostic register
255  */
256 #define MPI2_HOST_DIAGNOSTIC_OFFSET             (0x00000008)

258 #define MPI2_DIAG_BOOT_DEVICE_SELECT_MASK       (0x00001800)
259 #define MPI2_DIAG_BOOT_DEVICE_SELECT_DEFAULT    (0x00000000)
260 #define MPI2_DIAG_BOOT_DEVICE_SELECT_HCDW       (0x00000800)

262 #define MPI2_DIAG_CLEAR_FLASH_BAD_SIG           (0x00000400)
263 #define MPI2_DIAG_FORCE_HCB_ON_RESET            (0x00000200)
264 #define MPI2_DIAG_HCB_MODE                      (0x00000100)
265 #define MPI2_DIAG_DIAG_WRITE_ENABLE             (0x00000080)
266 #define MPI2_DIAG_FLASH_BAD_SIG                 (0x00000040)
267 #define MPI2_DIAG_RESET_HISTORY                 (0x00000020)
268 #define MPI2_DIAG_DIAG_RW_ENABLE                (0x00000010)
269 #define MPI2_DIAG_RESET_ADAPTER                 (0x00000004)
270 #define MPI2_DIAG_HOLD_IOC_RESET                (0x00000002)

272 /*
273  * Offsets for DiagRWData and address
274  */
275 #define MPI2_DIAG_RW_DATA_OFFSET                (0x00000010)
276 #define MPI2_DIAG_RW_ADDRESS_LOW_OFFSET         (0x00000014)
277 #define MPI2_DIAG_RW_ADDRESS_HIGH_OFFSET        (0x00000018)
```



```
279 /*
280  * Defines for the HostInterruptStatus register
281  */
282 #define MPI2_HOST_INTERRUPT_STATUS_OFFSET       (0x00000030)
283 #define MPI2_HIS_SYS2IOC_DB_STATUS              (0x80000000)
284 #define MPI2_HIS_IOP_DOORBELL_STATUS            MPI2_HIS_SYS2IOC_DB_STATUS
285 #define MPI2_HIS_RESET_IRQ_STATUS               (0x40000000)
286 #define MPI2_HIS_REPLY_DESCRIPTOR_INTERRUPT     (0x00000008)
287 #define MPI2_HIS_IOC2SYS_DB_STATUS              (0x00000001)
288 #define MPI2_HIS_DOORBELL_INTERRUPT             MPI2_HIS_IOC2SYS_DB_STATUS

290 /*
291  * Defines for the HostInterruptMask register
292  */
293 #define MPI2_HOST_INTERRUPT_MASK_OFFSET         (0x00000034)
294 #define MPI2_HIM_RESET_IRQ_MASK                 (0x40000000)
295 #define MPI2_HIM_REPLY_INT_MASK                 (0x00000008)
296 #define MPI2_HIM_RIM                            MPI2_HIM_REPLY_INT_MASK
297 #define MPI2_HIM_IOC2SYS_DB_MASK                (0x00000001)
298 #define MPI2_HIM_DIM                            MPI2_HIM_IOC2SYS_DB_MASK

300 /*
301  * Offsets for DCRData and address
302  */
303 #define MPI2_DCR_DATA_OFFSET                    (0x00000038)
304 #define MPI2_DCR_ADDRESS_OFFSET                 (0x0000003C)

306 /*
307  * Offset for the Reply Free Queue
308  */
309 #define MPI2_REPLY_FREE_HOST_INDEX_OFFSET       (0x00000048)

311 /*
312  * Defines for the Reply Descriptor Post Queue
280  * Offset for the Reply Descriptor Post Queue
313  */
314 #define MPI2_REPLY_POST_HOST_INDEX_OFFSET       (0x0000006C)
315 #define MPI2_REPLY_POST_HOST_INDEX_MASK         (0x00FFFFFF)
316 #define MPI2_RPHI_MSIX_INDEX_MASK               (0xFF000000)
317 #define MPI2_RPHI_MSIX_INDEX_SHIFT              (24)
318 #define MPI25_SUP_REPLY_POST_HOST_INDEX_OFFSET  (0x0000030C) /* MPI v2.5 only */


321 /*
322  * Defines for the HCBSize and address
323  */
324 #define MPI2_HCB_SIZE_OFFSET                    (0x00000074)
325 #define MPI2_HCB_SIZE_SIZE_MASK                 (0xFFFFF000)
326 #define MPI2_HCB_SIZE_HCB_ENABLE                (0x00000001)

328 #define MPI2_HCB_ADDRESS_LOW_OFFSET             (0x00000078)
329 #define MPI2_HCB_ADDRESS_HIGH_OFFSET            (0x0000007C)

331 /*
332  * Offsets for the Request Queue
333  */
334 #define MPI2_REQUEST_DESCRIPTOR_POST_LOW_OFFSET     (0x000000C0)
335 #define MPI2_REQUEST_DESCRIPTOR_POST_HIGH_OFFSET    (0x000000C4)


338 /* Hard Reset delay timings */
339 #define MPI2_HARD_RESET_PCIE_FIRST_READ_DELAY_MICRO_SEC     (50000)
340 #define MPI2_HARD_RESET_PCIE_RESET_READ_WINDOW_MICRO_SEC    (255000)
341 #define MPI2_HARD_RESET_PCIE_SECOND_READ_DELAY_MICRO_SEC    (256000)
```

```
/*****************************************************************************
*
*        Message Descriptors
*
*****************************************************************************/

/* Request Descriptors */

/* Default Request Descriptor */
typedef struct _MPI2_DEFAULT_REQUEST_DESCRIPTOR
{
    U8              RequestFlags;               /* 0x00 */
    U8              MSIxIndex;                  /* 0x01 */
    U16             SMID;                       /* 0x02 */
    U16             LMID;                       /* 0x04 */
    U16             DescriptorTypeDependent;    /* 0x06 */
} MPI2_DEFAULT_REQUEST_DESCRIPTOR,
  MPI2_POINTER PTR_MPI2_DEFAULT_REQUEST_DESCRIPTOR,
  Mpi2DefaultRequestDescriptor_t, MPI2_POINTER pMpi2DefaultRequestDescriptor_t;

/* defines for the RequestFlags field */
#define MPI2_REQ_DESCRIPT_FLAGS_TYPE_MASK               (0x0E)
#define MPI2_REQ_DESCRIPT_FLAGS_SCSI_IO                 (0x00)
#define MPI2_REQ_DESCRIPT_FLAGS_SCSI_TARGET             (0x02)
#define MPI2_REQ_DESCRIPT_FLAGS_HIGH_PRIORITY           (0x06)
#define MPI2_REQ_DESCRIPT_FLAGS_DEFAULT_TYPE            (0x08)
#define MPI2_REQ_DESCRIPT_FLAGS_RAID_ACCELERATOR        (0x0A)
#define MPI25_REQ_DESCRIPT_FLAGS_FAST_PATH_SCSI_IO      (0x0C)

#define MPI2_REQ_DESCRIPT_FLAGS_IOC_FIFO_MARKER (0x01)


/* High Priority Request Descriptor */
typedef struct _MPI2_HIGH_PRIORITY_REQUEST_DESCRIPTOR
{
    U8              RequestFlags;               /* 0x00 */
    U8              MSIxIndex;                  /* 0x01 */
    U16             SMID;                       /* 0x02 */
    U16             LMID;                       /* 0x04 */
    U16             Reserved1;                  /* 0x06 */
} MPI2_HIGH_PRIORITY_REQUEST_DESCRIPTOR,
______unchanged_portion_omitted_
  MPI2_POINTER PTR_MPI2_RAID_ACCEL_REQUEST_DESCRIPTOR,
  Mpi2RAIDAcceleratorRequestDescriptor_t,
  MPI2_POINTER pMpi2RAIDAcceleratorRequestDescriptor_t;


/* Fast Path SCSI IO Request Descriptor */
typedef MPI2_SCSI_IO_REQUEST_DESCRIPTOR
    MPI25_FP_SCSI_IO_REQUEST_DESCRIPTOR,
    MPI2_POINTER PTR_MPI25_FP_SCSI_IO_REQUEST_DESCRIPTOR,
    Mpi25FastPathSCSIIORequestDescriptor_t,
    MPI2_POINTER pMpi25FastPathSCSIIORequestDescriptor_t;


/* union of Request Descriptors */
typedef union _MPI2_REQUEST_DESCRIPTOR_UNION
{
    MPI2_DEFAULT_REQUEST_DESCRIPTOR             Default;
    MPI2_HIGH_PRIORITY_REQUEST_DESCRIPTOR       HighPriority;
    MPI2_SCSI_IO_REQUEST_DESCRIPTOR             SCSIIO;
    MPI2_SCSI_TARGET_REQUEST_DESCRIPTOR         SCSITarget;
    MPI2_RAID_ACCEL_REQUEST_DESCRIPTOR          RAIDAccelerator;
    MPI25_FP_SCSI_IO_REQUEST_DESCRIPTOR         FastPathSCSIIO;
    U64                                         Words;
} MPI2_REQUEST_DESCRIPTOR_UNION, MPI2_POINTER PTR_MPI2_REQUEST_DESCRIPTOR_UNION,
______unchanged_portion_omitted_
```



```
  Mpi2DefaultReplyDescriptor_t, MPI2_POINTER pMpi2DefaultReplyDescriptor_t;

/* defines for the ReplyFlags field */
#define MPI2_RPY_DESCRIPT_FLAGS_TYPE_MASK                   (0x0F)
#define MPI2_RPY_DESCRIPT_FLAGS_SCSI_IO_SUCCESS             (0x00)
#define MPI2_RPY_DESCRIPT_FLAGS_ADDRESS_REPLY               (0x01)
#define MPI2_RPY_DESCRIPT_FLAGS_TARGETASSIST_SUCCESS        (0x02)
#define MPI2_RPY_DESCRIPT_FLAGS_TARGET_COMMAND_BUFFER       (0x03)
#define MPI2_RPY_DESCRIPT_FLAGS_RAID_ACCELERATOR_SUCCESS    (0x05)
#define MPI25_RPY_DESCRIPT_FLAGS_FAST_PATH_SCSI_IO_SUCCESS  (0x06)
#define MPI2_RPY_DESCRIPT_FLAGS_UNUSED                      (0x0F)

/* values for marking a reply descriptor as unused */
#define MPI2_RPY_DESCRIPT_UNUSED_WORD0_MARK             (0xFFFFFFFF)
#define MPI2_RPY_DESCRIPT_UNUSED_WORD1_MARK             (0xFFFFFFFF)

/* Address Reply Descriptor */
typedef struct _MPI2_ADDRESS_REPLY_DESCRIPTOR
{
    U8              ReplyFlags;                 /* 0x00 */
    U8              MSIxIndex;                  /* 0x01 */
    U16             SMID;                       /* 0x02 */
    U32             ReplyFrameAddress;          /* 0x04 */
} MPI2_ADDRESS_REPLY_DESCRIPTOR, MPI2_POINTER PTR_MPI2_ADDRESS_REPLY_DESCRIPTOR,
______unchanged_portion_omitted_
  MPI2_POINTER PTR_MPI2_RAID_ACCELERATOR_SUCCESS_REPLY_DESCRIPTOR,
  Mpi2RAIDAcceleratorSuccessReplyDescriptor_t,
  MPI2_POINTER pMpi2RAIDAcceleratorSuccessReplyDescriptor_t;


/* Fast Path SCSI IO Success Reply Descriptor */
typedef MPI2_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR
    MPI25_FP_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR,
    MPI2_POINTER PTR_MPI25_FP_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR,
    Mpi25FastPathSCSIIOSuccessReplyDescriptor_t,
    MPI2_POINTER pMpi25FastPathSCSIIOSuccessReplyDescriptor_t;


/* union of Reply Descriptors */
typedef union _MPI2_REPLY_DESCRIPTORS_UNION
{
    MPI2_DEFAULT_REPLY_DESCRIPTOR                   Default;
    MPI2_ADDRESS_REPLY_DESCRIPTOR                   AddressReply;
    MPI2_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR           SCSIIOSuccess;
    MPI2_TARGETASSIST_SUCCESS_REPLY_DESCRIPTOR      TargetAssistSuccess;
    MPI2_TARGET_COMMAND_BUFFER_REPLY_DESCRIPTOR     TargetCommandBuffer;
    MPI2_RAID_ACCELERATOR_SUCCESS_REPLY_DESCRIPTOR  RAIDAcceleratorSuccess;
    MPI25_FP_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR       FastPathSCSIIOSuccess;
    U64                                             Words;
} MPI2_REPLY_DESCRIPTORS_UNION, MPI2_POINTER PTR_MPI2_REPLY_DESCRIPTORS_UNION,
  Mpi2ReplyDescriptorsUnion_t, MPI2_POINTER pMpi2ReplyDescriptorsUnion_t;



/*****************************************************************************
*
*        Message Functions
*             0x80 -> 0x8F reserved for private message use per product
*
*****************************************************************************/

#define MPI2_FUNCTION_SCSI_IO_REQUEST               (0x00) /* SCSI IO */
#define MPI2_FUNCTION_SCSI_TASK_MGMT                (0x01) /* SCSI Task Manageme
#define MPI2_FUNCTION_IOC_INIT                      (0x02) /* IOC Init */
#define MPI2_FUNCTION_IOC_FACTS                     (0x03) /* IOC Facts */
```

```
585 #define MPI2_FUNCTION_CONFIG                        (0x04) /* Configuration */
586 #define MPI2_FUNCTION_PORT_FACTS                    (0x05) /* Port Facts */
587 #define MPI2_FUNCTION_PORT_ENABLE                   (0x06) /* Port Enable */
588 #define MPI2_FUNCTION_EVENT_NOTIFICATION            (0x07) /* Event Notification
589 #define MPI2_FUNCTION_EVENT_ACK                     (0x08) /* Event Acknowledge
590 #define MPI2_FUNCTION_FW_DOWNLOAD                   (0x09) /* FW Download */
591 #define MPI2_FUNCTION_TARGET_ASSIST                 (0x0B) /* Target Assist */
592 #define MPI2_FUNCTION_TARGET_STATUS_SEND            (0x0C) /* Target Status Send
593 #define MPI2_FUNCTION_TARGET_MODE_ABORT             (0x0D) /* Target Mode Abort
594 #define MPI2_FUNCTION_FW_UPLOAD                     (0x12) /* FW Upload */
595 #define MPI2_FUNCTION_RAID_ACTION                   (0x15) /* RAID Action */
596 #define MPI2_FUNCTION_RAID_SCSI_IO_PASSTHROUGH      (0x16) /* SCSI IO RAID Passt
597 #define MPI2_FUNCTION_TOOLBOX                       (0x17) /* Toolbox */
598 #define MPI2_FUNCTION_SCSI_ENCLOSURE_PROCESSOR      (0x18) /* SCSI Enclosure Pro
599 #define MPI2_FUNCTION_SMP_PASSTHROUGH               (0x1A) /* SMP Passthrough */
600 #define MPI2_FUNCTION_SAS_IO_UNIT_CONTROL           (0x1B) /* SAS IO Unit Contro
601 #define MPI2_FUNCTION_SATA_PASSTHROUGH              (0x1C) /* SATA Passthrough *
602 #define MPI2_FUNCTION_DIAG_BUFFER_POST              (0x1D) /* Diagnostic Buffer
603 #define MPI2_FUNCTION_DIAG_RELEASE                  (0x1E) /* Diagnostic Release
604 #define MPI2_FUNCTION_TARGET_CMD_BUF_BASE_POST      (0x24) /* Target Command Buf
605 #define MPI2_FUNCTION_TARGET_CMD_BUF_LIST_POST      (0x25) /* Target Command Buf
606 #define MPI2_FUNCTION_RAID_ACCELERATOR              (0x2C) /* RAID Accelerator *
607 #define MPI2_FUNCTION_HOST_BASED_DISCOVERY_ACTION   (0x2F) /* Host Based Discove
608 #define MPI2_FUNCTION_PWR_MGMT_CONTROL              (0x30) /* Power Management C
609 #define MPI2_FUNCTION_SEND_HOST_MESSAGE             (0x31) /* Send Host Message
610 #define MPI2_FUNCTION_MIN_PRODUCT_SPECIFIC          (0xF0) /* beginning of produ
611 #define MPI2_FUNCTION_MAX_PRODUCT_SPECIFIC          (0xFF) /* end of product-spe


615 /* Doorbell functions */
616 #define MPI2_FUNCTION_IOC_MESSAGE_UNIT_RESET        (0x40)
552 /* #define MPI2_FUNCTION_IO_UNIT_RESET                 (0x41) */
617 #define MPI2_FUNCTION_HANDSHAKE                     (0x42)


620 /****************************************************************************
621 *
622 *        IOC Status Values
623 *
624 ****************************************************************************/

626 /* mask for IOCStatus status value */
627 #define MPI2_IOCSTATUS_MASK                     (0x7FFF)

629 /****************************************************************************
630 *  Common IOCStatus values for all replies
631 ****************************************************************************/

633 #define MPI2_IOCSTATUS_SUCCESS                      (0x0000)
634 #define MPI2_IOCSTATUS_INVALID_FUNCTION             (0x0001)
635 #define MPI2_IOCSTATUS_BUSY                         (0x0002)
636 #define MPI2_IOCSTATUS_INVALID_SGL                  (0x0003)
637 #define MPI2_IOCSTATUS_INTERNAL_ERROR               (0x0004)
638 #define MPI2_IOCSTATUS_INVALID_VPID                 (0x0005)
639 #define MPI2_IOCSTATUS_INSUFFICIENT_RESOURCES       (0x0006)
640 #define MPI2_IOCSTATUS_INVALID_FIELD                (0x0007)
641 #define MPI2_IOCSTATUS_INVALID_STATE                (0x0008)
642 #define MPI2_IOCSTATUS_OP_STATE_NOT_SUPPORTED       (0x0009)

644 /****************************************************************************
645 *  Config IOCStatus values
646 ****************************************************************************/

648 #define MPI2_IOCSTATUS_CONFIG_INVALID_ACTION        (0x0020)
649 #define MPI2_IOCSTATUS_CONFIG_INVALID_TYPE          (0x0021)
```



```
650 #define MPI2_IOCSTATUS_CONFIG_INVALID_PAGE          (0x0022)
651 #define MPI2_IOCSTATUS_CONFIG_INVALID_DATA          (0x0023)
652 #define MPI2_IOCSTATUS_CONFIG_NO_DEFAULTS           (0x0024)
653 #define MPI2_IOCSTATUS_CONFIG_CANT_COMMIT           (0x0025)

655 /****************************************************************************
656 *  SCSI IO Reply
657 ****************************************************************************/

659 #define MPI2_IOCSTATUS_SCSI_RECOVERED_ERROR         (0x0040)
660 #define MPI2_IOCSTATUS_SCSI_INVALID_DEVHANDLE       (0x0042)
661 #define MPI2_IOCSTATUS_SCSI_DEVICE_NOT_THERE        (0x0043)
662 #define MPI2_IOCSTATUS_SCSI_DATA_OVERRUN            (0x0044)
663 #define MPI2_IOCSTATUS_SCSI_DATA_UNDERRUN           (0x0045)
664 #define MPI2_IOCSTATUS_SCSI_IO_DATA_ERROR           (0x0046)
665 #define MPI2_IOCSTATUS_SCSI_PROTOCOL_ERROR          (0x0047)
666 #define MPI2_IOCSTATUS_SCSI_TASK_TERMINATED         (0x0048)
667 #define MPI2_IOCSTATUS_SCSI_RESIDUAL_MISMATCH       (0x0049)
668 #define MPI2_IOCSTATUS_SCSI_TASK_MGMT_FAILED        (0x004A)
669 #define MPI2_IOCSTATUS_SCSI_IOC_TERMINATED          (0x004B)
670 #define MPI2_IOCSTATUS_SCSI_EXT_TERMINATED          (0x004C)

672 /****************************************************************************
673 *  For use by SCSI Initiator and SCSI Target end-to-end data protection
674 ****************************************************************************/

676 #define MPI2_IOCSTATUS_EEDP_GUARD_ERROR             (0x004D)
677 #define MPI2_IOCSTATUS_EEDP_REF_TAG_ERROR           (0x004E)
678 #define MPI2_IOCSTATUS_EEDP_APP_TAG_ERROR           (0x004F)

680 /****************************************************************************
681 *  SCSI Target values
682 ****************************************************************************/

684 #define MPI2_IOCSTATUS_TARGET_INVALID_IO_INDEX      (0x0062)
685 #define MPI2_IOCSTATUS_TARGET_ABORTED               (0x0063)
686 #define MPI2_IOCSTATUS_TARGET_NO_CONN_RETRYABLE     (0x0064)
687 #define MPI2_IOCSTATUS_TARGET_NO_CONNECTION         (0x0065)
688 #define MPI2_IOCSTATUS_TARGET_XFER_COUNT_MISMATCH   (0x006A)
689 #define MPI2_IOCSTATUS_TARGET_DATA_OFFSET_ERROR     (0x006D)
690 #define MPI2_IOCSTATUS_TARGET_TOO_MUCH_WRITE_DATA   (0x006E)
691 #define MPI2_IOCSTATUS_TARGET_IU_TOO_SHORT          (0x006F)
692 #define MPI2_IOCSTATUS_TARGET_ACK_NAK_TIMEOUT       (0x0070)
693 #define MPI2_IOCSTATUS_TARGET_NAK_RECEIVED          (0x0071)

695 /****************************************************************************
696 *  Serial Attached SCSI values
697 ****************************************************************************/

699 #define MPI2_IOCSTATUS_SAS_SMP_REQUEST_FAILED       (0x0090)
700 #define MPI2_IOCSTATUS_SAS_SMP_DATA_OVERRUN         (0x0091)

702 /****************************************************************************
703 *  Diagnostic Buffer Post / Diagnostic Release values
704 ****************************************************************************/

706 #define MPI2_IOCSTATUS_DIAGNOSTIC_RELEASED          (0x00A0)

708 /****************************************************************************
709 *  RAID Accelerator values
710 ****************************************************************************/

712 #define MPI2_IOCSTATUS_RAID_ACCEL_ERROR             (0x00B0)

714 /****************************************************************************
715 *  IOCStatus flag to indicate that log info is available
```

```
 716 *****************************************************************************/

 718 #define MPI2_IOCSTATUS_FLAG_LOG_INFO_AVAILABLE      (0x8000)

 720 /****************************************************************************
 721 *  IOCLogInfo Types
 722 ****************************************************************************/

 724 #define MPI2_IOCLOGINFO_TYPE_MASK               (0xF0000000)
 725 #define MPI2_IOCLOGINFO_TYPE_SHIFT              (28)
 726 #define MPI2_IOCLOGINFO_TYPE_NONE               (0x0)
 727 #define MPI2_IOCLOGINFO_TYPE_SCSI               (0x1)
 728 #define MPI2_IOCLOGINFO_TYPE_FC                 (0x2)
 729 #define MPI2_IOCLOGINFO_TYPE_SAS                (0x3)
 730 #define MPI2_IOCLOGINFO_TYPE_ISCSI              (0x4)
 731 #define MPI2_IOCLOGINFO_LOG_DATA_MASK           (0x0FFFFFFF)


 734 /****************************************************************************
 735 *
 736 *        Standard Message Structures
 737 *
 738 ****************************************************************************/

 740 /****************************************************************************
 741 * Request Message Header for all request messages
 742 ****************************************************************************/

 744 typedef struct _MPI2_REQUEST_HEADER
 745 {
 746     U16             FunctionDependent1;         /* 0x00 */
 747     U8              ChainOffset;                /* 0x02 */
 748     U8              Function;                   /* 0x03 */
 749     U16             FunctionDependent2;         /* 0x04 */
 750     U8              FunctionDependent3;         /* 0x06 */
 751     U8              MsgFlags;                   /* 0x07 */
 752     U8              VP_ID;                      /* 0x08 */
 753     U8              VF_ID;                      /* 0x09 */
 754     U16             Reserved1;                  /* 0x0A */
 755 } MPI2_REQUEST_HEADER, MPI2_POINTER PTR_MPI2_REQUEST_HEADER,
_____unchanged_portion_omitted_
 840   Mpi2SGESimpleUnion_t, MPI2_POINTER pMpi2SGESimpleUnion_t;


 843 /****************************************************************************
 844 *  MPI Chain Element structures - for MPI v2.0 products only
 780 *  MPI Chain Element structures
 845 ****************************************************************************/

 847 typedef struct _MPI2_SGE_CHAIN32
 848 {
 849     U16                     Length;
 850     U8                      NextChainOffset;
 851     U8                      Flags;
 852     U32                     Address;
 853 } MPI2_SGE_CHAIN32, MPI2_POINTER PTR_MPI2_SGE_CHAIN32,
_____unchanged_portion_omitted_
 876   Mpi2SGEChainUnion_t, MPI2_POINTER pMpi2SGEChainUnion_t;


 879 /****************************************************************************
 880 *  MPI Transaction Context Element structures - for MPI v2.0 products only
 816 *  MPI Transaction Context Element structures
 881 ****************************************************************************/

 883 typedef struct _MPI2_SGE_TRANSACTION32
```



```
 884 {
 885     U8                      Reserved;
 886     U8                      ContextSize;
 887     U8                      DetailsLength;
 888     U8                      Flags;
 889     U32                     TransactionContext[1];
 890     U32                     TransactionDetails[1];
 891 } MPI2_SGE_TRANSACTION32, MPI2_POINTER PTR_MPI2_SGE_TRANSACTION32,
_____unchanged_portion_omitted_
 942   Mpi2SGETransactionUnion_t, MPI2_POINTER pMpi2SGETransactionUnion_t;


 945 /****************************************************************************
 946 *  MPI SGE union for IO SGL's - for MPI v2.0 products only
 882 *  MPI SGE union for IO SGL's
 947 ****************************************************************************/

 949 typedef struct _MPI2_MPI_SGE_IO_UNION
 950 {
 951     union
 952     {
 953         MPI2_SGE_SIMPLE_UNION   Simple;
 954         MPI2_SGE_CHAIN_UNION    Chain;
 955     } u;
 956 } MPI2_MPI_SGE_IO_UNION, MPI2_POINTER PTR_MPI2_MPI_SGE_IO_UNION,
 957   Mpi2MpiSGEIOUnion_t, MPI2_POINTER pMpi2MpiSGEIOUnion_t;


 960 /****************************************************************************
 961 *  MPI SGE union for SGL's with Simple and Transaction elements - for MPI v2.0 p
 897 *  MPI SGE union for SGL's with Simple and Transaction elements
 962 ****************************************************************************/

 964 typedef struct _MPI2_SGE_TRANS_SIMPLE_UNION
 965 {
 966     union
 967     {
 968         MPI2_SGE_SIMPLE_UNION       Simple;
 969         MPI2_SGE_TRANSACTION_UNION  Transaction;
 970     } u;
 971 } MPI2_SGE_TRANS_SIMPLE_UNION, MPI2_POINTER PTR_MPI2_SGE_TRANS_SIMPLE_UNION,
_____unchanged_portion_omitted_
 988   Mpi2MpiSgeUnion_t, MPI2_POINTER pMpi2MpiSgeUnion_t;


 991 /****************************************************************************
 992 *  MPI SGE field definition and masks
 993 ****************************************************************************/

 995 /* Flags field bit definitions */

 997 #define MPI2_SGE_FLAGS_LAST_ELEMENT             (0x80)
 998 #define MPI2_SGE_FLAGS_END_OF_BUFFER            (0x40)
 999 #define MPI2_SGE_FLAGS_ELEMENT_TYPE_MASK        (0x30)
1000 #define MPI2_SGE_FLAGS_LOCAL_ADDRESS            (0x08)
1001 #define MPI2_SGE_FLAGS_DIRECTION                (0x04)
1002 #define MPI2_SGE_FLAGS_ADDRESS_SIZE             (0x02)
1003 #define MPI2_SGE_FLAGS_END_OF_LIST              (0x01)

1005 #define MPI2_SGE_FLAGS_SHIFT                    (24)

1007 #define MPI2_SGE_LENGTH_MASK                    (0x00FFFFFF)
1008 #define MPI2_SGE_CHAIN_LENGTH_MASK              (0x0000FFFF)

1010 /* Element Type */
```

```
#define MPI2_SGE_FLAGS_TRANSACTION_ELEMENT      (0x00) /* for MPI v2.0 products
#define MPI2_SGE_FLAGS_TRANSACTION_ELEMENT      (0x00)
#define MPI2_SGE_FLAGS_SIMPLE_ELEMENT           (0x10)
#define MPI2_SGE_FLAGS_CHAIN_ELEMENT            (0x30) /* for MPI v2.0 products
#define MPI2_SGE_FLAGS_CHAIN_ELEMENT            (0x30)
#define MPI2_SGE_FLAGS_ELEMENT_MASK             (0x30)

/* Address location */

#define MPI2_SGE_FLAGS_SYSTEM_ADDRESS           (0x00)

/* Direction */

#define MPI2_SGE_FLAGS_IOC_TO_HOST              (0x00)
#define MPI2_SGE_FLAGS_HOST_TO_IOC              (0x04)

#define MPI2_SGE_FLAGS_DEST                     (MPI2_SGE_FLAGS_IOC_TO_HOST)
#define MPI2_SGE_FLAGS_SOURCE                   (MPI2_SGE_FLAGS_HOST_TO_IOC)

/* Address Size */

#define MPI2_SGE_FLAGS_32_BIT_ADDRESSING        (0x00)
#define MPI2_SGE_FLAGS_64_BIT_ADDRESSING        (0x02)

/* Context Size */

#define MPI2_SGE_FLAGS_32_BIT_CONTEXT           (0x00)
#define MPI2_SGE_FLAGS_64_BIT_CONTEXT           (0x02)
#define MPI2_SGE_FLAGS_96_BIT_CONTEXT           (0x04)
#define MPI2_SGE_FLAGS_128_BIT_CONTEXT          (0x06)

#define MPI2_SGE_CHAIN_OFFSET_MASK              (0x00FF0000)
#define MPI2_SGE_CHAIN_OFFSET_SHIFT             (16)

/****************************************************************************
*  MPI SGE operation Macros
****************************************************************************/

/* SIMPLE FlagsLength manipulations... */
#define MPI2_SGE_SET_FLAGS(f)           ((U32)(f) << MPI2_SGE_FLAGS_SHIFT)
#define MPI2_SGE_GET_FLAGS(f)           (((f) & ~MPI2_SGE_LENGTH_MASK) >> MPI2_SG
#define MPI2_SGE_LENGTH(f)              ((f) & MPI2_SGE_LENGTH_MASK)
#define MPI2_SGE_CHAIN_LENGTH(f)        ((f) & MPI2_SGE_CHAIN_LENGTH_MASK)

#define MPI2_SGE_SET_FLAGS_LENGTH(f,l) (MPI2_SGE_SET_FLAGS(f) | MPI2_SGE_LENGTH(

#define MPI2_pSGE_GET_FLAGS(psg)            MPI2_SGE_GET_FLAGS((psg)->FlagsLengt
#define MPI2_pSGE_GET_LENGTH(psg)           MPI2_SGE_LENGTH((psg)->FlagsLength)
#define MPI2_pSGE_SET_FLAGS_LENGTH(psg,f,l) (psg)->FlagsLength = MPI2_SGE_SET_FL

/* CAUTION - The following are READ-MODIFY-WRITE! */
#define MPI2_pSGE_SET_FLAGS(psg,f)      (psg)->FlagsLength |= MPI2_SGE_SET_FLAGS
#define MPI2_pSGE_SET_LENGTH(psg,l)     (psg)->FlagsLength |= MPI2_SGE_LENGTH(l)

#define MPI2_GET_CHAIN_OFFSET(x)    ((x & MPI2_SGE_CHAIN_OFFSET_MASK) >> MPI2_SG


/****************************************************************************
*
*        Fusion-MPT IEEE Scatter Gather Elements
*
****************************************************************************/

/****************************************************************************
*  IEEE Simple Element structures
****************************************************************************/
```



```
/* MPI2_IEEE_SGE_SIMPLE32 is for MPI v2.0 products only */
typedef struct _MPI2_IEEE_SGE_SIMPLE32
{
    U32                     Address;
    U32                     FlagsLength;
} MPI2_IEEE_SGE_SIMPLE32, MPI2_POINTER PTR_MPI2_IEEE_SGE_SIMPLE32,
_____unchanged_portion_omitted_
  Mpi2IeeeSgeSimpleUnion_t, MPI2_POINTER pMpi2IeeeSgeSimpleUnion_t;


/****************************************************************************
*  IEEE Chain Element structures
****************************************************************************/

/* MPI2_IEEE_SGE_CHAIN32 is for MPI v2.0 products only */
typedef MPI2_IEEE_SGE_SIMPLE32  MPI2_IEEE_SGE_CHAIN32;

/* MPI2_IEEE_SGE_CHAIN64 is for MPI v2.0 products only */
typedef MPI2_IEEE_SGE_SIMPLE64  MPI2_IEEE_SGE_CHAIN64;

typedef union _MPI2_IEEE_SGE_CHAIN_UNION
{
    MPI2_IEEE_SGE_CHAIN32   Chain32;
    MPI2_IEEE_SGE_CHAIN64   Chain64;
} MPI2_IEEE_SGE_CHAIN_UNION, MPI2_POINTER PTR_MPI2_IEEE_SGE_CHAIN_UNION,
  Mpi2IeeeSgeChainUnion_t, MPI2_POINTER pMpi2IeeeSgeChainUnion_t;

/* MPI25_IEEE_SGE_CHAIN64 is for MPI v2.5 products only */
typedef struct _MPI25_IEEE_SGE_CHAIN64
{
    U64                     Address;
    U32                     Length;
    U16                     Reserved1;
    U8                      NextChainOffset;
    U8                      Flags;
} MPI25_IEEE_SGE_CHAIN64, MPI2_POINTER PTR_MPI25_IEEE_SGE_CHAIN64,
  Mpi25IeeeSgeChain64_t, MPI2_POINTER pMpi25IeeeSgeChain64_t;


/****************************************************************************
*  All IEEE SGE types union
****************************************************************************/

/* MPI2_IEEE_SGE_UNION is for MPI v2.0 products only */
typedef struct _MPI2_IEEE_SGE_UNION
{
    union
    {
        MPI2_IEEE_SGE_SIMPLE_UNION  Simple;
        MPI2_IEEE_SGE_CHAIN_UNION   Chain;
    } u;
} MPI2_IEEE_SGE_UNION, MPI2_POINTER PTR_MPI2_IEEE_SGE_UNION,
  Mpi2IeeeSgeUnion_t, MPI2_POINTER pMpi2IeeeSgeUnion_t;


/****************************************************************************
*  IEEE SGE union for IO SGL's
****************************************************************************/

typedef union _MPI25_SGE_IO_UNION
{
    MPI2_IEEE_SGE_SIMPLE64      IeeeSimple;
    MPI25_IEEE_SGE_CHAIN64      IeeeChain;
} MPI25_SGE_IO_UNION, MPI2_POINTER PTR_MPI25_SGE_IO_UNION,
  Mpi25SGEIOUnion_t, MPI2_POINTER pMpi25SGEIOUnion_t;
```

```
1160 /*****************************************************************************
1161 *  IEEE SGE field definitions and masks
1162 *****************************************************************************/

1164 /* Flags field bit definitions */

1166 #define MPI2_IEEE_SGE_FLAGS_ELEMENT_TYPE_MASK   (0x80)
1167 #define MPI25_IEEE_SGE_FLAGS_END_OF_LIST        (0x40)

1169 #define MPI2_IEEE32_SGE_FLAGS_SHIFT             (24)

1171 #define MPI2_IEEE32_SGE_LENGTH_MASK             (0x00FFFFFF)

1173 /* Element Type */

1175 #define MPI2_IEEE_SGE_FLAGS_SIMPLE_ELEMENT      (0x00)
1176 #define MPI2_IEEE_SGE_FLAGS_CHAIN_ELEMENT       (0x80)

1178 /* Data Location Address Space */

1180 #define MPI2_IEEE_SGE_FLAGS_ADDR_MASK           (0x03)
1181 #define MPI2_IEEE_SGE_FLAGS_SYSTEM_ADDR         (0x00) /* for MPI v2.0, use in I
1182 #define MPI2_IEEE_SGE_FLAGS_IOCDDR_ADDR         (0x01) /* use in IEEE Simple Ele
1086 #define MPI2_IEEE_SGE_FLAGS_SYSTEM_ADDR         (0x00)
1087 #define MPI2_IEEE_SGE_FLAGS_IOCDDR_ADDR         (0x01)
1183 #define MPI2_IEEE_SGE_FLAGS_IOCPLB_ADDR         (0x02)
1184 #define MPI2_IEEE_SGE_FLAGS_IOCPLBNTA_ADDR      (0x03) /* for MPI v2.0, use in I
1185 #define MPI2_IEEE_SGE_FLAGS_SYSTEMPLBPCI_ADDR   (0x03) /* use in MPI v2.0 IEEE C
1186 #define MPI2_IEEE_SGE_FLAGS_SYSTEMPLBCPI_ADDR   (MPI2_IEEE_SGE_FLAGS_SYSTEMPLBPC
1089 #define MPI2_IEEE_SGE_FLAGS_IOCPLBNTA_ADDR      (0x03)

1188 /*****************************************************************************
1189 *  IEEE SGE operation Macros
1190 *****************************************************************************/

1192 /* SIMPLE FlagsLength manipulations... */
1193 #define MPI2_IEEE32_SGE_SET_FLAGS(f)     ((U32)(f) << MPI2_IEEE32_SGE_FLAGS_SHIF
1194 #define MPI2_IEEE32_SGE_GET_FLAGS(f)     (((f) & ~MPI2_IEEE32_SGE_LENGTH_MASK) >
1195 #define MPI2_IEEE32_SGE_LENGTH(f)        ((f) & MPI2_IEEE32_SGE_LENGTH_MASK)

1197 #define MPI2_IEEE32_SGE_SET_FLAGS_LENGTH(f, l)      (MPI2_IEEE32_SGE_SET_FLAGS(f

1199 #define MPI2_IEEE32_pSGE_GET_FLAGS(psg)             MPI2_IEEE32_SGE_GET_FLAGS((p
1200 #define MPI2_IEEE32_pSGE_GET_LENGTH(psg)            MPI2_IEEE32_SGE_LENGTH((psg)
1201 #define MPI2_IEEE32_pSGE_SET_FLAGS_LENGTH(psg,f,l)  (psg)->FlagsLength = MPI2_IE

1203 /* CAUTION - The following are READ-MODIFY-WRITE! */
1204 #define MPI2_IEEE32_pSGE_SET_FLAGS(psg,f)    (psg)->FlagsLength |= MPI2_IEEE32_S
1205 #define MPI2_IEEE32_pSGE_SET_LENGTH(psg,l)   (psg)->FlagsLength |= MPI2_IEEE32_S



1209 /*****************************************************************************
1210 *
1211 *        Fusion-MPT MPI/IEEE Scatter Gather Unions
1212 *
1213 *****************************************************************************/

1215 typedef union _MPI2_SIMPLE_SGE_UNION
1216 {
1217     MPI2_SGE_SIMPLE_UNION       MpiSimple;
1218     MPI2_IEEE_SGE_SIMPLE_UNION  IeeeSimple;
```



```
1219 } MPI2_SIMPLE_SGE_UNION, MPI2_POINTER PTR_MPI2_SIMPLE_SGE_UNION,
_____unchanged_portion_omitted_
1230   Mpi2SGEIOUnion_t, MPI2_POINTER pMpi2SGEIOUnion_t;


1233 /*****************************************************************************
1234 *
1235 *  Values for SGLFlags field, used in many request messages with an SGL
1236 *
1237 *****************************************************************************/

1239 /* values for MPI SGL Data Location Address Space subfield */
1240 #define MPI2_SGLFLAGS_ADDRESS_SPACE_MASK            (0x0C)
1241 #define MPI2_SGLFLAGS_SYSTEM_ADDRESS_SPACE          (0x00)
1242 #define MPI2_SGLFLAGS_IOCDDR_ADDRESS_SPACE          (0x04)
1243 #define MPI2_SGLFLAGS_IOCPLB_ADDRESS_SPACE          (0x08)
1244 #define MPI2_SGLFLAGS_IOCPLBNTA_ADDRESS_SPACE       (0x0C)
1245 /* values for SGL Type subfield */
1246 #define MPI2_SGLFLAGS_SGL_TYPE_MASK                 (0x03)
1247 #define MPI2_SGLFLAGS_SGL_TYPE_MPI                  (0x00)
1248 #define MPI2_SGLFLAGS_SGL_TYPE_IEEE32               (0x01) /* MPI v2.0 products
1153 #define MPI2_SGLFLAGS_SGL_TYPE_IEEE32               (0x01)
1249 #define MPI2_SGLFLAGS_SGL_TYPE_IEEE64               (0x02)


1252 #endif
```

```
**********************************************************
  158147 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_cnfg.h
NEX-1888 upstream
**********************************************************
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 */

/*
 *          Name:  mpi2_cnfg.h
 *         Title:  MPI Configuration messages and pages
 *  Creation Date:  November 10, 2006
 *
 *    mpi2_cnfg.h Version:  02.00.27
 *    mpi2_cnfg.h Version:  02.00.12
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-04-07  02.00.01  Added defines for SAS IO Unit Page 2 PhyFlags.
 *                      Added Manufacturing Page 11.
 *                      Added MPI2_SAS_EXPANDER0_FLAGS_CONNECTOR_END_DEVICE
 *                      define.
 *  06-26-07  02.00.02  Adding generic structure for product-specific
 *                      Manufacturing pages: MPI2_CONFIG_PAGE_MANUFACTURING_PS.
 *                      Rework of BIOS Page 2 configuration page.
 *                      Fixed MPI2_BIOSPAGE2_BOOT_DEVICE to be a union of the
 *                      forms.
 *                      Added configuration pages IOC Page 8 and Driver
 *                      Persistent Mapping Page 0.
 *  08-31-07  02.00.03  Modified configuration pages dealing with Integrated
 *                      RAID (Manufacturing Page 4, RAID Volume Pages 0 and 1,
 *                      RAID Physical Disk Pages 0 and 1, RAID Configuration
 *                      Page 0).
 *                      Added new value for AccessStatus field of SAS Device
 *                      Page 0 (_SATA_NEEDS_INITIALIZATION).
 *  10-31-07  02.00.04  Added missing SEPDevHandle field to
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *  12-18-07  02.00.05  Modified IO Unit Page 0 to use 32-bit version fields for
 *                      NVDATA.
 *                      Modified IOC Page 7 to use masks and added field for
 *                      SASBroadcastPrimitiveMasks.
 *                      Added MPI2_CONFIG_PAGE_BIOS_4.
 *                      Added MPI2_CONFIG_PAGE_LOG_0.
 *  02-29-08  02.00.06  Modified various names to make them 32-character unique.
 *                      Added SAS Device IDs.
 *                      Updated Integrated RAID configuration pages including
 *                      Manufacturing Page 4, IOC Page 6, and RAID Configuration
 *                      Page 0.
 *  05-21-08  02.00.07  Added define MPI2_MANPAGE4_MIX_SSD_SAS_SATA.
 *                      Added define MPI2_MANPAGE4_PHYSDISK_128MB_COERCION.
 *                      Fixed define MPI2_IOCPAGE8_FLAGS_ENCLOSURE_SLOT_MAPPING.
 *                      Added missing MaxNumRoutedSasAddresses field to
```

```
 *                      MPI2_CONFIG_PAGE_EXPANDER_0.
 *                      Added SAS Port Page 0.
 *                      Modified structure layout for
 *                      MPI2_CONFIG_PAGE_DRIVER_MAPPING_0.
 *  06-27-08  02.00.08  Changed MPI2_CONFIG_PAGE_RD_PDISK_1 to use
 *                      MPI2_RAID_PHYS_DISK1_PATH_MAX to size the array.
 *  10-02-08  02.00.09  Changed MPI2_RAID_PGAD_CONFIGNUM_MASK from 0x0000FFFF
 *                      to 0x000000FF.
 *                      Added two new values for the Physical Disk Coercion Size
 *                      bits in the Flags field of Manufacturing Page 4.
 *                      Added product-specific Manufacturing pages 16 to 31.
 *                      Modified Flags bits for controlling write cache on SATA
 *                      drives in IO Unit Page 1.
 *                      Added new bit to AdditionalControlFlags of SAS IO Unit
 *                      Page 1 to control Invalid Topology Correction.
 *                      Added additional defines for RAID Volume Page 0
 *                      VolumeStatusFlags field.
 *                      Modified meaning of RAID Volume Page 0 VolumeSettings
 *                      define for auto-configure of hot-swap drives.
 *                      Added SupportedPhysDisks field to RAID Volume Page 1 and
 *                      added related defines.
 *                      Added PhysDiskAttributes field (and related defines) to
 *                      RAID Physical Disk Page 0.
 *                      Added MPI2_SAS_PHYINFO_PHY_VACANT define.
 *                      Added three new DiscoveryStatus bits for SAS IO Unit
 *                      Page 0 and SAS Expander Page 0.
 *                      Removed multiplexing information from SAS IO Unit pages.
 *                      Added BootDeviceWaitTime field to SAS IO Unit Page 4.
 *                      Removed Zone Address Resolved bit from PhyInfo and from
 *                      Expander Page 0 Flags field.
 *                      Added two new AccessStatus values to SAS Device Page 0
 *                      for indicating routing problems. Added 3 reserved words
 *                      to this page.
 *  01-19-09  02.00.10  Fixed defines for GPIOVal field of IO Unit Page 3.
 *                      Inserted missing reserved field into structure for IOC
 *                      Page 6.
 *                      Added more pending task bits to RAID Volume Page 0
 *                      VolumeStatusFlags defines.
 *                      Added MPI2_PHYSDISK0_STATUS_FLAG_NOT_CERTIFIED define.
 *                      Added a new DiscoveryStatus bit for SAS IO Unit Page 0
 *                      and SAS Expander Page 0 to flag a downstream initiator
 *                      when in simplified routing mode.
 *                      Removed SATA Init Failure defines for DiscoveryStatus
 *                      fields of SAS IO Unit Page 0 and SAS Expander Page 0.
 *                      Added MPI2_SAS_DEVICE0_ASTATUS_DEVICE_BLOCKED define.
 *                      Added PortGroups, DmaGroup, and ControlGroup fields to
 *                      SAS Device Page 0.
 *  05-06-09  02.00.11  Added structures and defines for IO Unit Page 5 and IO
 *                      Unit Page 6.
 *                      Added expander reduced functionality data to SAS
 *                      Expander Page 0.
 *                      Added SAS PHY Page 2 and SAS PHY Page 3.
 *  07-30-09  02.00.12  Added IO Unit Page 7.
 *                      Added new device ids.
 *                      Added SAS IO Unit Page 5.
 *                      Added partial and slumber power management capable flags
 *                      to SAS Device Page 0 Flags field.
 *                      Added PhyInfo defines for power condition.
 *                      Added Ethernet configuration pages.
 *  10-28-09  02.00.13  Added MPI2_IOUNITPAGE1_ENABLE_HOST_BASED_DISCOVERY.
 *                      Added SAS PHY Page 4 structure and defines.
 *  02-10-10  02.00.14  Modified the comments for the configuration page
 *                      structures that contain an array of data. The host
 *                      should use the "count" field in the page data (e.g. the
 *                      NumPhys field) to determine the number of valid elements
 *                      in the array.
```



```
 *                      Added/modified some MPI2_MFGPAGE_DEVID_SAS defines.
 *                      Added PowerManagementCapabilities to IO Unit Page 7.
 *                      Added PortWidthModGroup field to
 *                      MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_6 and related defines.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_7 and related defines.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_8 and related defines.
 *  05-12-10  02.00.15  Added MPI2_RAIDVOL0_STATUS_FLAG_VOL_NOT_CONSISTENT
 *                      define.
 *                      Added MPI2_PHYSDISK0_INCOMPATIBLE_MEDIA_TYPE define.
 *                      Added MPI2_SAS_NEG_LINK_RATE_UNSUPPORTED_PHY define.
 *  08-11-10  02.00.16  Removed IO Unit Page 1 device path (multi-pathing)
 *                      defines.
 *  11-10-10  02.00.17  Added ReceptacleID field (replacing Reserved1) to
 *                      MPI2_MANPAGE7_CONNECTOR_INFO and reworked defines for
 *                      the Pinout field.
 *                      Added BoardTemperature and BoardTemperatureUnits fields
 *                      to MPI2_CONFIG_PAGE_IO_UNIT_7.
 *                      Added MPI2_CONFIG_EXTPAGETYPE_EXT_MANUFACTURING define
 *                      and MPI2_CONFIG_PAGE_EXT_MAN_PS structure.
 *  02-23-11  02.00.18  Added ProxyVF_ID field to MPI2_CONFIG_REQUEST.
 *                      Added IO Unit Page 8, IO Unit Page 9,
 *                      and IO Unit Page 10.
 *                      Added SASNotifyPrimitiveMasks field to
 *                      MPI2_CONFIG_PAGE_IOC_7.
 *  03-09-11  02.00.19  Fixed IO Unit Page 10 (to match the spec).
 *  05-25-11  02.00.20  Cleaned up a few comments.
 *  08-24-11  02.00.21  Marked the IO Unit Page 7 PowerManagementCapabilities
 *                      for PCIe link as obsolete.
 *                      Added SpinupFlags field containing a Disable Spin-up bit
 *                      to the MPI2_SAS_IOUNIT4_SPINUP_GROUP fields of SAS IO
 *                      Unit Page 4.
 *  11-18-11  02.00.22  Added define MPI2_IOCPAGE6_CAP_FLAGS_4K_SECTORS_SUPPORT.
 *                      Added UEFIVersion field to BIOS Page 1 and defined new
 *                      BiosOptions bits.
 *                      Incorporating additions for MPI v2.5.
 *  11-27-12  02.00.23  Added MPI2_MANPAGE7_FLAG_EVENTREPLAY_SLOT_ORDER.
 *                      Added MPI2_BIOSPAGE1_OPTIONS_MASK_OEM_ID.
 *  12-20-12  02.00.24  Marked MPI2_SASIOUNIT1_CONTROL_CLEAR_AFFILIATION as
 *                      obsolete for MPI v2.5 and later.
 *                      Added some defines for 12G SAS speeds.
 *  04-09-13  02.00.25  Added MPI2_IOUNITPAGE1_ATA_SECURITY_FREEZE_LOCK.
 *                      Fixed MPI2_IOUNITPAGE5_DMA_CAP_MASK_MAX_REQUESTS to
 *                      match the specification.
 *  08-19-13  02.00.26  Added reserved words to MPI2_CONFIG_PAGE_IO_UNIT_7 for
 *                      future use.
 *  12-05-13  02.00.27  Added MPI2_MANPAGE7_FLAG_BASE_ENCLOSURE_LEVEL for
 *                      MPI2_CONFIG_PAGE_MAN_7.
 *                      Added EnclosureLevel and ConnectorName fields to
 *                      MPI2_CONFIG_PAGE_SAS_DEV_0.
 *                      Added MPI2_SAS_DEVICE0_FLAGS_ENCL_LEVEL_VALID for
 *                      MPI2_CONFIG_PAGE_SAS_DEV_0.
 *                      Added EnclosureLevel field to
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *                      Added MPI2_SAS_ENCLS0_FLAGS_ENCL_LEVEL_VALID for
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *  --------------------------------------------------------------------------
 */

#ifndef MPI2_CNFG_H
#define MPI2_CNFG_H

/*****************************************************************************
*   Configuration Page Header and defines
*****************************************************************************/
```

```
 217 /* Config Page Header */
 218 typedef struct _MPI2_CONFIG_PAGE_HEADER
 219 {
 220     U8                 PageVersion;               /* 0x00 */
 221     U8                 PageLength;                /* 0x01 */
 222     U8                 PageNumber;                /* 0x02 */
 223     U8                 PageType;                  /* 0x03 */
 224 } MPI2_CONFIG_PAGE_HEADER, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_HEADER,
_____unchanged_portion_omitted_
 258   Mpi2ConfigPageExtendedHeaderUnion, MPI2_POINTER pMpi2ConfigPageExtendedHeaderU


 261 /* PageType field values */
 262 #define MPI2_CONFIG_PAGEATTR_READ_ONLY             (0x00)
 263 #define MPI2_CONFIG_PAGEATTR_CHANGEABLE            (0x10)
 264 #define MPI2_CONFIG_PAGEATTR_PERSISTENT            (0x20)
 265 #define MPI2_CONFIG_PAGEATTR_MASK                  (0xF0)

 267 #define MPI2_CONFIG_PAGETYPE_IO_UNIT               (0x00)
 268 #define MPI2_CONFIG_PAGETYPE_IOC                   (0x01)
 269 #define MPI2_CONFIG_PAGETYPE_BIOS                  (0x02)
 270 #define MPI2_CONFIG_PAGETYPE_RAID_VOLUME           (0x08)
 271 #define MPI2_CONFIG_PAGETYPE_MANUFACTURING         (0x09)
 272 #define MPI2_CONFIG_PAGETYPE_RAID_PHYSDISK         (0x0A)
 273 #define MPI2_CONFIG_PAGETYPE_EXTENDED              (0x0F)
 274 #define MPI2_CONFIG_PAGETYPE_MASK                  (0x0F)

 276 #define MPI2_CONFIG_TYPENUM_MASK                   (0x0FFF)


 279 /* ExtPageType field values */
 280 #define MPI2_CONFIG_EXTPAGETYPE_SAS_IO_UNIT        (0x10)
 281 #define MPI2_CONFIG_EXTPAGETYPE_SAS_EXPANDER       (0x11)
 282 #define MPI2_CONFIG_EXTPAGETYPE_SAS_DEVICE         (0x12)
 283 #define MPI2_CONFIG_EXTPAGETYPE_SAS_PHY            (0x13)
 284 #define MPI2_CONFIG_EXTPAGETYPE_LOG                (0x14)
 285 #define MPI2_CONFIG_EXTPAGETYPE_ENCLOSURE          (0x15)
 286 #define MPI2_CONFIG_EXTPAGETYPE_RAID_CONFIG        (0x16)
 287 #define MPI2_CONFIG_EXTPAGETYPE_DRIVER_MAPPING     (0x17)
 288 #define MPI2_CONFIG_EXTPAGETYPE_SAS_PORT           (0x18)
 289 #define MPI2_CONFIG_EXTPAGETYPE_ETHERNET           (0x19)
 290 #define MPI2_CONFIG_EXTPAGETYPE_EXT_MANUFACTURING  (0x1A)


 293 /*****************************************************************************
 294 *   PageAddress defines
 295 *****************************************************************************/

 297 /* RAID Volume PageAddress format */
 298 #define MPI2_RAID_VOLUME_PGAD_FORM_MASK            (0xF0000000)
 299 #define MPI2_RAID_VOLUME_PGAD_FORM_GET_NEXT_HANDLE (0x00000000)
 300 #define MPI2_RAID_VOLUME_PGAD_FORM_HANDLE          (0x10000000)

 302 #define MPI2_RAID_VOLUME_PGAD_HANDLE_MASK          (0x0000FFFF)


 305 /* RAID Physical Disk PageAddress format */
 306 #define MPI2_PHYSDISK_PGAD_FORM_MASK                  (0xF0000000)
 307 #define MPI2_PHYSDISK_PGAD_FORM_GET_NEXT_PHYSDISKNUM  (0x00000000)
 308 #define MPI2_PHYSDISK_PGAD_FORM_PHYSDISKNUM           (0x10000000)
 309 #define MPI2_PHYSDISK_PGAD_FORM_DEVHANDLE             (0x20000000)

 311 #define MPI2_PHYSDISK_PGAD_PHYSDISKNUM_MASK           (0x000000FF)
 312 #define MPI2_PHYSDISK_PGAD_DEVHANDLE_MASK             (0x0000FFFF)
```



```
 315 /* SAS Expander PageAddress format */
 316 #define MPI2_SAS_EXPAND_PGAD_FORM_MASK             (0xF0000000)
 317 #define MPI2_SAS_EXPAND_PGAD_FORM_GET_NEXT_HNDL    (0x00000000)
 318 #define MPI2_SAS_EXPAND_PGAD_FORM_HNDL_PHY_NUM     (0x10000000)
 319 #define MPI2_SAS_EXPAND_PGAD_FORM_HNDL             (0x20000000)

 321 #define MPI2_SAS_EXPAND_PGAD_HANDLE_MASK           (0x0000FFFF)
 322 #define MPI2_SAS_EXPAND_PGAD_PHYNUM_MASK           (0x00FF0000)
 323 #define MPI2_SAS_EXPAND_PGAD_PHYNUM_SHIFT          (16)


 326 /* SAS Device PageAddress format */
 327 #define MPI2_SAS_DEVICE_PGAD_FORM_MASK             (0xF0000000)
 328 #define MPI2_SAS_DEVICE_PGAD_FORM_GET_NEXT_HANDLE  (0x00000000)
 329 #define MPI2_SAS_DEVICE_PGAD_FORM_HANDLE           (0x20000000)

 331 #define MPI2_SAS_DEVICE_PGAD_HANDLE_MASK           (0x0000FFFF)


 334 /* SAS PHY PageAddress format */
 335 #define MPI2_SAS_PHY_PGAD_FORM_MASK                (0xF0000000)
 336 #define MPI2_SAS_PHY_PGAD_FORM_PHY_NUMBER          (0x00000000)
 337 #define MPI2_SAS_PHY_PGAD_FORM_PHY_TBL_INDEX       (0x10000000)

 339 #define MPI2_SAS_PHY_PGAD_PHY_NUMBER_MASK          (0x000000FF)
 340 #define MPI2_SAS_PHY_PGAD_PHY_TBL_INDEX_MASK       (0x0000FFFF)


 343 /* SAS Port PageAddress format */
 344 #define MPI2_SASPORT_PGAD_FORM_MASK                (0xF0000000)
 345 #define MPI2_SASPORT_PGAD_FORM_GET_NEXT_PORT       (0x00000000)
 346 #define MPI2_SASPORT_PGAD_FORM_PORT_NUM            (0x10000000)

 348 #define MPI2_SASPORT_PGAD_PORTNUMBER_MASK          (0x00000FFF)


 351 /* SAS Enclosure PageAddress format */
 352 #define MPI2_SAS_ENCLOS_PGAD_FORM_MASK             (0xF0000000)
 353 #define MPI2_SAS_ENCLOS_PGAD_FORM_GET_NEXT_HANDLE  (0x00000000)
 354 #define MPI2_SAS_ENCLOS_PGAD_FORM_HANDLE           (0x10000000)

 356 #define MPI2_SAS_ENCLOS_PGAD_HANDLE_MASK           (0x0000FFFF)


 359 /* RAID Configuration PageAddress format */
 360 #define MPI2_RAID_PGAD_FORM_MASK                   (0xF0000000)
 361 #define MPI2_RAID_PGAD_FORM_GET_NEXT_CONFIGNUM     (0x00000000)
 362 #define MPI2_RAID_PGAD_FORM_CONFIGNUM              (0x10000000)
 363 #define MPI2_RAID_PGAD_FORM_ACTIVE_CONFIG          (0x20000000)

 365 #define MPI2_RAID_PGAD_CONFIGNUM_MASK              (0x000000FF)


 368 /* Driver Persistent Mapping PageAddress format */
 369 #define MPI2_DPM_PGAD_FORM_MASK                    (0xF0000000)
 370 #define MPI2_DPM_PGAD_FORM_ENTRY_RANGE             (0x00000000)

 372 #define MPI2_DPM_PGAD_ENTRY_COUNT_MASK             (0x0FFF0000)
 373 #define MPI2_DPM_PGAD_ENTRY_COUNT_SHIFT            (16)
 374 #define MPI2_DPM_PGAD_START_ENTRY_MASK             (0x0000FFFF)


 377 /* Ethernet PageAddress format */
 378 #define MPI2_ETHERNET_PGAD_FORM_MASK               (0xF0000000)
 379 #define MPI2_ETHERNET_PGAD_FORM_IF_NUM             (0x00000000)
```

```
#define MPI2_ETHERNET_PGAD_IF_NUMBER_MASK           (0x000000FF)



/*****************************************************************************
*   Configuration messages
*****************************************************************************/

/* Configuration Request Message */
typedef struct _MPI2_CONFIG_REQUEST
{
    U8                      Action;                 /* 0x00 */
    U8                      SGLFlags;               /* 0x01 */
    U8                      ChainOffset;            /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     ExtPageLength;          /* 0x04 */
    U8                      ExtPageType;            /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved1;              /* 0x0A */
    U8                      Reserved2;              /* 0x0C */
    U8                      ProxyVF_ID;             /* 0x0D */
    U16                     Reserved4;              /* 0x0E */
    U32                     Reserved2;              /* 0x0C */
    U32                     Reserved3;              /* 0x10 */
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x14 */
    U32                     PageAddress;            /* 0x18 */
    MPI2_SGE_IO_UNION       PageBufferSGE;          /* 0x1C */
} MPI2_CONFIG_REQUEST, MPI2_POINTER PTR_MPI2_CONFIG_REQUEST,
  Mpi2ConfigRequest_t, MPI2_POINTER pMpi2ConfigRequest_t;

/* values for the Action field */
#define MPI2_CONFIG_ACTION_PAGE_HEADER              (0x00)
#define MPI2_CONFIG_ACTION_PAGE_READ_CURRENT        (0x01)
#define MPI2_CONFIG_ACTION_PAGE_WRITE_CURRENT       (0x02)
#define MPI2_CONFIG_ACTION_PAGE_DEFAULT             (0x03)
#define MPI2_CONFIG_ACTION_PAGE_WRITE_NVRAM         (0x04)
#define MPI2_CONFIG_ACTION_PAGE_READ_DEFAULT        (0x05)
#define MPI2_CONFIG_ACTION_PAGE_READ_NVRAM          (0x06)
#define MPI2_CONFIG_ACTION_PAGE_GET_CHANGEABLE      (0x07)

/* use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */
/* values for SGLFlags field are in the SGL section of mpi2.h */


/* Config Reply Message */
typedef struct _MPI2_CONFIG_REPLY
{
    U8                      Action;                 /* 0x00 */
    U8                      SGLFlags;               /* 0x01 */
    U8                      MsgLength;              /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     ExtPageLength;          /* 0x04 */
    U8                      ExtPageType;            /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved1;              /* 0x0A */
    U16                     Reserved2;              /* 0x0C */
    U16                     IOCStatus;              /* 0x0E */
    U32                     IOCLogInfo;             /* 0x10 */
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x14 */
} MPI2_CONFIG_REPLY, MPI2_POINTER PTR_MPI2_CONFIG_REPLY,
  Mpi2ConfigReply_t, MPI2_POINTER pMpi2ConfigReply_t;
```



```
/*****************************************************************************
*
*               C o n f i g u r a t i o n    P a g e s
*
*****************************************************************************/

/*****************************************************************************
*   Manufacturing Config pages
*****************************************************************************/

#define MPI2_MFGPAGE_VENDORID_LSI                   (0x1000)

/* MPI v2.0 SAS products */
/* SAS */
#define MPI2_MFGPAGE_DEVID_SAS2004                  (0x0070)
#define MPI2_MFGPAGE_DEVID_SAS2008                  (0x0072)
#define MPI2_MFGPAGE_DEVID_SAS2108_1                (0x0074)
#define MPI2_MFGPAGE_DEVID_SAS2108_2                (0x0076)
#define MPI2_MFGPAGE_DEVID_SAS2108_3                (0x0077)
#define MPI2_MFGPAGE_DEVID_SAS2116_1                (0x0064)
#define MPI2_MFGPAGE_DEVID_SAS2116_2                (0x0065)

#define MPI2_MFGPAGE_DEVID_SSS6200                  (0x007E)

#define MPI2_MFGPAGE_DEVID_SAS2208_1                (0x0080)
#define MPI2_MFGPAGE_DEVID_SAS2208_2                (0x0081)
#define MPI2_MFGPAGE_DEVID_SAS2208_3                (0x0082)
#define MPI2_MFGPAGE_DEVID_SAS2208_4                (0x0083)
#define MPI2_MFGPAGE_DEVID_SAS2208_5                (0x0084)
#define MPI2_MFGPAGE_DEVID_SAS2208_6                (0x0085)
#define MPI2_MFGPAGE_DEVID_SAS2308_1                (0x0086)
#define MPI2_MFGPAGE_DEVID_SAS2308_2                (0x0087)
#define MPI2_MFGPAGE_DEVID_SAS2308_3                (0x006E)
#define MPI2_MFGPAGE_DEVID_SAS2208_7                (0x0086)
#define MPI2_MFGPAGE_DEVID_SAS2208_8                (0x0087)

/* MPI v2.5 SAS products */
#define MPI25_MFGPAGE_DEVID_SAS3004                 (0x0096)
#define MPI25_MFGPAGE_DEVID_SAS3008                 (0x0097)
#define MPI25_MFGPAGE_DEVID_SAS3108_1               (0x0090)
#define MPI25_MFGPAGE_DEVID_SAS3108_2               (0x0091)
#define MPI25_MFGPAGE_DEVID_SAS3108_5               (0x0094)
#define MPI25_MFGPAGE_DEVID_SAS3108_6               (0x0095)



/* Manufacturing Page 0 */

typedef struct _MPI2_CONFIG_PAGE_MAN_0
{
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x00 */
    U8                      ChipName[16];           /* 0x04 */
    U8                      ChipRevision[8];        /* 0x14 */
    U8                      BoardName[16];          /* 0x1C */
    U8                      BoardAssembly[16];      /* 0x2C */
    U8                      BoardTracerNumber[16];  /* 0x3C */
} MPI2_CONFIG_PAGE_MAN_0,
      unchanged_portion_omitted
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_MAN_4,
  Mpi2ManufacturingPage4_t, MPI2_POINTER pMpi2ManufacturingPage4_t;

#define MPI2_MANUFACTURING4_PAGEVERSION             (0x0A)
```

```
 621 /* Manufacturing Page 4 Flags field */
 622 #define MPI2_MANPAGE4_METADATA_SIZE_MASK                (0x00030000)
 623 #define MPI2_MANPAGE4_METADATA_512MB                    (0x00000000)

 625 #define MPI2_MANPAGE4_MIX_SSD_SAS_SATA                  (0x00008000)
 626 #define MPI2_MANPAGE4_MIX_SSD_AND_NON_SSD               (0x00004000)
 627 #define MPI2_MANPAGE4_HIDE_PHYSDISK_NON_IR              (0x00002000)

 629 #define MPI2_MANPAGE4_MASK_PHYSDISK_COERCION            (0x00001C00)
 630 #define MPI2_MANPAGE4_PHYSDISK_COERCION_1GB             (0x00000000)
 631 #define MPI2_MANPAGE4_PHYSDISK_128MB_COERCION           (0x00000400)
 632 #define MPI2_MANPAGE4_PHYSDISK_ADAPTIVE_COERCION        (0x00000800)
 633 #define MPI2_MANPAGE4_PHYSDISK_ZERO_COERCION            (0x00000C00)

 635 #define MPI2_MANPAGE4_MASK_BAD_BLOCK_MARKING            (0x00000300)
 636 #define MPI2_MANPAGE4_DEFAULT_BAD_BLOCK_MARKING         (0x00000000)
 637 #define MPI2_MANPAGE4_TABLE_BAD_BLOCK_MARKING           (0x00000100)
 638 #define MPI2_MANPAGE4_WRITE_LONG_BAD_BLOCK_MARKING      (0x00000200)

 640 #define MPI2_MANPAGE4_FORCE_OFFLINE_FAILOVER            (0x00000080)
 641 #define MPI2_MANPAGE4_RAID10_DISABLE                    (0x00000040)
 642 #define MPI2_MANPAGE4_RAID1E_DISABLE                    (0x00000020)
 643 #define MPI2_MANPAGE4_RAID1_DISABLE                     (0x00000010)
 644 #define MPI2_MANPAGE4_RAID0_DISABLE                     (0x00000008)
 645 #define MPI2_MANPAGE4_IR_MODEPAGE8_DISABLE              (0x00000004)
 646 #define MPI2_MANPAGE4_IM_RESYNC_CACHE_ENABLE            (0x00000002)
 647 #define MPI2_MANPAGE4_IR_NO_MIX_SAS_SATA                (0x00000001)


 650 /* Manufacturing Page 5 */

 652 /*
 653  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 654  * one and check the value returned for NumPhys at runtime.
 586  * one and check Header.PageLength or NumPhys at runtime.
 655  */
 656 #ifndef MPI2_MAN_PAGE_5_PHY_ENTRIES
 657 #define MPI2_MAN_PAGE_5_PHY_ENTRIES        (1)
 658 #endif

 660 typedef struct _MPI2_MANUFACTURING5_ENTRY
 661 {
 662     U64                                 WWID;           /* 0x00 */
 663     U64                                 DeviceName;     /* 0x08 */
 664 } MPI2_MANUFACTURING5_ENTRY, MPI2_POINTER PTR_MPI2_MANUFACTURING5_ENTRY,
_____unchanged_portion_omitted_
 690   MPI2_POINTER PTR_MPI2_CONFIG_PAGE_MAN_6,
 691   Mpi2ManufacturingPage6_t, MPI2_POINTER pMpi2ManufacturingPage6_t;

 693 #define MPI2_MANUFACTURING6_PAGEVERSION                 (0x00)


 696 /* Manufacturing Page 7 */

 698 typedef struct _MPI2_MANPAGE7_CONNECTOR_INFO
 699 {
 700     U32                         Pinout;                 /* 0x00 */
 701     U8                          Connector[16];          /* 0x04 */
 702     U8                          Location;               /* 0x14 */
 703     U8                          ReceptacleID;           /* 0x15 */
 635     U8                          Reserved1;              /* 0x15 */
 704     U16                         Slot;                   /* 0x16 */
 705     U32                         Reserved2;              /* 0x18 */
 706 } MPI2_MANPAGE7_CONNECTOR_INFO, MPI2_POINTER PTR_MPI2_MANPAGE7_CONNECTOR_INFO,
 707   Mpi2ManPage7ConnectorInfo_t, MPI2_POINTER pMpi2ManPage7ConnectorInfo_t;
```



```
 709 /* defines for the Pinout field */
 710 #define MPI2_MANPAGE7_PINOUT_LANE_MASK                  (0x0000FF00)
 711 #define MPI2_MANPAGE7_PINOUT_LANE_SHIFT                 (8)
 642 #define MPI2_MANPAGE7_PINOUT_SFF_8484_L4                (0x00080000)
 643 #define MPI2_MANPAGE7_PINOUT_SFF_8484_L3                (0x00040000)
 644 #define MPI2_MANPAGE7_PINOUT_SFF_8484_L2                (0x00020000)
 645 #define MPI2_MANPAGE7_PINOUT_SFF_8484_L1                (0x00010000)
 646 #define MPI2_MANPAGE7_PINOUT_SFF_8470_L4                (0x00000800)
 647 #define MPI2_MANPAGE7_PINOUT_SFF_8470_L3                (0x00000400)
 648 #define MPI2_MANPAGE7_PINOUT_SFF_8470_L2                (0x00000200)
 649 #define MPI2_MANPAGE7_PINOUT_SFF_8470_L1                (0x00000100)
 650 #define MPI2_MANPAGE7_PINOUT_SFF_8482                   (0x00000002)
 651 #define MPI2_MANPAGE7_PINOUT_CONNECTION_UNKNOWN         (0x00000001)

 713 #define MPI2_MANPAGE7_PINOUT_TYPE_MASK                  (0x000000FF)
 714 #define MPI2_MANPAGE7_PINOUT_TYPE_UNKNOWN               (0x00)
 715 #define MPI2_MANPAGE7_PINOUT_SATA_SINGLE                (0x01)
 716 #define MPI2_MANPAGE7_PINOUT_SFF_8482                   (0x02)
 717 #define MPI2_MANPAGE7_PINOUT_SFF_8486                   (0x03)
 718 #define MPI2_MANPAGE7_PINOUT_SFF_8484                   (0x04)
 719 #define MPI2_MANPAGE7_PINOUT_SFF_8087                   (0x05)
 720 #define MPI2_MANPAGE7_PINOUT_SFF_8643_4I                (0x06)
 721 #define MPI2_MANPAGE7_PINOUT_SFF_8643_8I                (0x07)
 722 #define MPI2_MANPAGE7_PINOUT_SFF_8470                   (0x08)
 723 #define MPI2_MANPAGE7_PINOUT_SFF_8088                   (0x09)
 724 #define MPI2_MANPAGE7_PINOUT_SFF_8644_4X                (0x0A)
 725 #define MPI2_MANPAGE7_PINOUT_SFF_8644_8X                (0x0B)
 726 #define MPI2_MANPAGE7_PINOUT_SFF_8644_16X               (0x0C)
 727 #define MPI2_MANPAGE7_PINOUT_SFF_8436                   (0x0D)

 729 /* defines for the Location field */
 730 #define MPI2_MANPAGE7_LOCATION_UNKNOWN                  (0x01)
 731 #define MPI2_MANPAGE7_LOCATION_INTERNAL                 (0x02)
 732 #define MPI2_MANPAGE7_LOCATION_EXTERNAL                 (0x04)
 733 #define MPI2_MANPAGE7_LOCATION_SWITCHABLE               (0x08)
 734 #define MPI2_MANPAGE7_LOCATION_AUTO                     (0x10)
 735 #define MPI2_MANPAGE7_LOCATION_NOT_PRESENT              (0x20)
 736 #define MPI2_MANPAGE7_LOCATION_NOT_CONNECTED            (0x80)

 738 /*
 739  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 740  * one and check the value returned for NumPhys at runtime.
 664  * one and check NumPhys at runtime.
 741  */
 742 #ifndef MPI2_MANPAGE7_CONNECTOR_INFO_MAX
 743 #define MPI2_MANPAGE7_CONNECTOR_INFO_MAX  (1)
 744 #endif

 746 typedef struct _MPI2_CONFIG_PAGE_MAN_7
 747 {
 748     MPI2_CONFIG_PAGE_HEADER         Header;             /* 0x00 */
 749     U32                             Reserved1;          /* 0x04 */
 750     U32                             Reserved2;          /* 0x08 */
 751     U32                             Flags;              /* 0x0C */
 752     U8                              EnclosureName[16];  /* 0x10 */
 753     U8                              NumPhys;            /* 0x20 */
 754     U8                              Reserved3;          /* 0x21 */
 755     U16                             Reserved4;          /* 0x22 */
 756     MPI2_MANPAGE7_CONNECTOR_INFO    ConnectorInfo[MPI2_MANPAGE7_CONNECTOR_INFO_M
 757 } MPI2_CONFIG_PAGE_MAN_7,
 758   MPI2_POINTER PTR_MPI2_CONFIG_PAGE_MAN_7,
 759   Mpi2ManufacturingPage7_t, MPI2_POINTER pMpi2ManufacturingPage7_t;

 761 #define MPI2_MANUFACTURING7_PAGEVERSION                 (0x01)
 685 #define MPI2_MANUFACTURING7_PAGEVERSION                 (0x00)
```

```
763 /* defines for the Flags field */
764 #define MPI2_MANPAGE7_FLAG_BASE_ENCLOSURE_LEVEL         (0x00000008)
765 #define MPI2_MANPAGE7_FLAG_EVENTREPLAY_SLOT_ORDER       (0x00000002)
766 #define MPI2_MANPAGE7_FLAG_USE_SLOT_INFO                (0x00000001)


769 /*
770  * Generic structure to use for product-specific manufacturing pages
771  * (currently Manufacturing Page 8 through Manufacturing Page 31).
772  */

774 typedef struct _MPI2_CONFIG_PAGE_MAN_PS
775 {
776     MPI2_CONFIG_PAGE_HEADER         Header;             /* 0x00 */
777     U32                             ProductSpecificInfo;/* 0x04 */
778 } MPI2_CONFIG_PAGE_MAN_PS,
      unchanged_portion_omitted_
833   Mpi2IOUnitPage1_t, MPI2_POINTER pMpi2IOUnitPage1_t;

835 #define MPI2_IOUNITPAGE1_PAGEVERSION                    (0x04)

837 /* IO Unit Page 1 Flags defines */
838 #define MPI2_IOUNITPAGE1_ATA_SECURITY_FREEZE_LOCK       (0x00004000)
839 #define MPI25_IOUNITPAGE1_NEW_DEVICE_FAST_PATH_DISABLE  (0x00002000)
840 #define MPI25_IOUNITPAGE1_DISABLE_FAST_PATH             (0x00001000)
841 #define MPI2_IOUNITPAGE1_ENABLE_HOST_BASED_DISCOVERY    (0x00000800)
842 #define MPI2_IOUNITPAGE1_MASK_SATA_WRITE_CACHE          (0x00000600)
843 #define MPI2_IOUNITPAGE1_SATA_WRITE_CACHE_SHIFT         (9)
844 #define MPI2_IOUNITPAGE1_ENABLE_SATA_WRITE_CACHE        (0x00000000)
845 #define MPI2_IOUNITPAGE1_DISABLE_SATA_WRITE_CACHE       (0x00000200)
846 #define MPI2_IOUNITPAGE1_UNCHANGED_SATA_WRITE_CACHE     (0x00000400)
847 #define MPI2_IOUNITPAGE1_NATIVE_COMMAND_Q_DISABLE       (0x00000100)
848 #define MPI2_IOUNITPAGE1_DISABLE_IR                     (0x00000040)
849 #define MPI2_IOUNITPAGE1_DISABLE_TASK_SET_FULL_HANDLING (0x00000020)
850 #define MPI2_IOUNITPAGE1_IR_USE_STATIC_VOLUME_ID        (0x00000004)
768 #define MPI2_IOUNITPAGE1_MULTI_PATHING                  (0x00000002)
769 #define MPI2_IOUNITPAGE1_SINGLE_PATHING                 (0x00000000)


853 /* IO Unit Page 3 */

855 /*
856  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
857  * one and check the value returned for GPIOCount at runtime.
776  * one and check Header.PageLength at runtime.
858  */
859 #ifndef MPI2_IO_UNIT_PAGE_3_GPIO_VAL_MAX
860 #define MPI2_IO_UNIT_PAGE_3_GPIO_VAL_MAX    (1)
861 #endif

863 typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_3
864 {
865     MPI2_CONFIG_PAGE_HEADER Header;                             /* 0x00 */
866     U8                      GPIOCount;                          /* 0x04 */
867     U8                      Reserved1;                          /* 0x05 */
868     U16                     Reserved2;                          /* 0x06 */
869     U16                     GPIOVal[MPI2_IO_UNIT_PAGE_3_GPIO_VAL_MAX];/* 0x08 */
870 } MPI2_CONFIG_PAGE_IO_UNIT_3, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_3,
871   Mpi2IOUnitPage3_t, MPI2_POINTER pMpi2IOUnitPage3_t;

873 #define MPI2_IOUNITPAGE3_PAGEVERSION                    (0x01)

875 /* defines for IO Unit Page 3 GPIOVal field */
876 #define MPI2_IOUNITPAGE3_GPIO_FUNCTION_MASK             (0xFFFC)
877 #define MPI2_IOUNITPAGE3_GPIO_FUNCTION_SHIFT            (2)
878 #define MPI2_IOUNITPAGE3_GPIO_SETTING_OFF               (0x0000)
```



```
879 #define MPI2_IOUNITPAGE3_GPIO_SETTING_ON                (0x0001)


882 /* IO Unit Page 5 */

884 /*
885  * Upper layer code (drivers, utilities, etc.) should leave this define set to
886  * one and check the value returned for NumDmaEngines at runtime.
805  * one and check Header.PageLength or NumDmaEngines at runtime.
887  */
888 #ifndef MPI2_IOUNITPAGE5_DMAENGINE_ENTRIES
889 #define MPI2_IOUNITPAGE5_DMAENGINE_ENTRIES      (1)
890 #endif

892 typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_5
893 {
894     MPI2_CONFIG_PAGE_HEADER Header;                                 /* 0x00
895     U64                     RaidAcceleratorBufferBaseAddress;       /* 0x04
896     U64                     RaidAcceleratorBufferSize;              /* 0x0C
897     U64                     RaidAcceleratorControlBaseAddress;      /* 0x14
898     U8                      RAControlSize;                          /* 0x1C
899     U8                      NumDmaEngines;                          /* 0x1D
900     U8                      RAMinControlSize;                       /* 0x1E
901     U8                      RAMaxControlSize;                       /* 0x1F
902     U32                     Reserved1;                              /* 0x20
903     U32                     Reserved2;                              /* 0x24
904     U32                     Reserved3;                              /* 0x28
905     U32                     DmaEngineCapabilities[MPI2_IOUNITPAGE5_DMAENGINE_ENT
906 } MPI2_CONFIG_PAGE_IO_UNIT_5, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_5,
907   Mpi2IOUnitPage5_t, MPI2_POINTER pMpi2IOUnitPage5_t;

909 #define MPI2_IOUNITPAGE5_PAGEVERSION                    (0x00)

911 /* defines for IO Unit Page 5 DmaEngineCapabilities field */
912 #define MPI2_IOUNITPAGE5_DMA_CAP_MASK_MAX_REQUESTS      (0xFFFF0000)
831 #define MPI2_IOUNITPAGE5_DMA_CAP_MASK_MAX_REQUESTS      (0xFF00)
913 #define MPI2_IOUNITPAGE5_DMA_CAP_SHIFT_MAX_REQUESTS     (16)

915 #define MPI2_IOUNITPAGE5_DMA_CAP_EEDP                   (0x0008)
916 #define MPI2_IOUNITPAGE5_DMA_CAP_PARITY_GENERATION      (0x0004)
917 #define MPI2_IOUNITPAGE5_DMA_CAP_HASHING                (0x0002)
918 #define MPI2_IOUNITPAGE5_DMA_CAP_ENCRYPTION             (0x0001)


921 /* IO Unit Page 6 */

923 typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_6
924 {
925     MPI2_CONFIG_PAGE_HEADER Header;                                 /* 0x00 */
926     U16                     Flags;                                  /* 0x04 */
927     U8                      RAHostControlSize;                      /* 0x06 */
928     U8                      Reserved0;                              /* 0x07 */
929     U64                     RaidAcceleratorHostControlBaseAddress;  /* 0x08 */
930     U32                     Reserved1;                              /* 0x10 */
931     U32                     Reserved2;                              /* 0x14 */
932     U32                     Reserved3;                              /* 0x18 */
933 } MPI2_CONFIG_PAGE_IO_UNIT_6, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_6,
934   Mpi2IOUnitPage6_t, MPI2_POINTER pMpi2IOUnitPage6_t;

936 #define MPI2_IOUNITPAGE6_PAGEVERSION                    (0x00)

938 /* defines for IO Unit Page 6 Flags field */
939 #define MPI2_IOUNITPAGE6_FLAGS_ENABLE_RAID_ACCELERATOR  (0x0001)


942 /* IO Unit Page 7 */
```

```
 944 typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_7
 945 {
 946     MPI2_CONFIG_PAGE_HEADER Header;                         /* 0x00 */
 947     U8                      CurrentPowerMode;               /* 0x04 */ /
 948     U8                      PreviousPowerMode;              /* 0x05 */ /
 866     U16                     Reserved1;                      /* 0x04 */
 949     U8                      PCIeWidth;                      /* 0x06 */
 950     U8                      PCIeSpeed;                      /* 0x07 */
 951     U32                     ProcessorState;                 /* 0x08 */
 952     U32                     PowerManagementCapabilities;    /* 0x0C */
 870     U32                     Reserved2;                      /* 0x0C */
 953     U16                     IOCTemperature;                 /* 0x10 */
 954     U8                      IOCTemperatureUnits;            /* 0x12 */
 955     U8                      IOCSpeed;                       /* 0x13 */
 956     U16                     BoardTemperature;               /* 0x14 */
 957     U8                      BoardTemperatureUnits;          /* 0x16 */
 958     U8                      Reserved3;                      /* 0x17 */
 959     U32                     Reserved4;                      /* 0x18 */
 960     U32                     Reserved5;                      /* 0x1C */
 961     U32                     Reserved6;                      /* 0x20 */
 962     U32                     Reserved7;                      /* 0x24 */
 874     U32                     Reserved3;                      /* 0x14 */
 963 } MPI2_CONFIG_PAGE_IO_UNIT_7, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_7,
 964   Mpi2IOUnitPage7_t, MPI2_POINTER pMpi2IOUnitPage7_t;

 966 #define MPI2_IOUNITPAGE7_PAGEVERSION                (0x04)
 878 #define MPI2_IOUNITPAGE7_PAGEVERSION                (0x00)

 968 /* defines for IO Unit Page 7 CurrentPowerMode and PreviousPowerMode fields */
 969 #define MPI25_IOUNITPAGE7_PM_INIT_MASK              (0xC0)
 970 #define MPI25_IOUNITPAGE7_PM_INIT_UNAVAILABLE       (0x00)
 971 #define MPI25_IOUNITPAGE7_PM_INIT_HOST              (0x40)
 972 #define MPI25_IOUNITPAGE7_PM_INIT_IO_UNIT           (0x80)
 973 #define MPI25_IOUNITPAGE7_PM_INIT_PCIE_DPA          (0xC0)

 975 #define MPI25_IOUNITPAGE7_PM_MODE_MASK              (0x07)
 976 #define MPI25_IOUNITPAGE7_PM_MODE_UNAVAILABLE       (0x00)
 977 #define MPI25_IOUNITPAGE7_PM_MODE_UNKNOWN           (0x01)
 978 #define MPI25_IOUNITPAGE7_PM_MODE_FULL_POWER        (0x04)
 979 #define MPI25_IOUNITPAGE7_PM_MODE_REDUCED_POWER     (0x05)
 980 #define MPI25_IOUNITPAGE7_PM_MODE_STANDBY           (0x06)


 983 /* defines for IO Unit Page 7 PCIeWidth field */
 984 #define MPI2_IOUNITPAGE7_PCIE_WIDTH_X1              (0x01)
 985 #define MPI2_IOUNITPAGE7_PCIE_WIDTH_X2              (0x02)
 986 #define MPI2_IOUNITPAGE7_PCIE_WIDTH_X4              (0x04)
 987 #define MPI2_IOUNITPAGE7_PCIE_WIDTH_X8              (0x08)

 989 /* defines for IO Unit Page 7 PCIeSpeed field */
 990 #define MPI2_IOUNITPAGE7_PCIE_SPEED_2_5_GBPS        (0x00)
 991 #define MPI2_IOUNITPAGE7_PCIE_SPEED_5_0_GBPS        (0x01)
 992 #define MPI2_IOUNITPAGE7_PCIE_SPEED_8_0_GBPS        (0x02)

 994 /* defines for IO Unit Page 7 ProcessorState field */
 995 #define MPI2_IOUNITPAGE7_PSTATE_MASK_SECOND         (0x0000000F)
 996 #define MPI2_IOUNITPAGE7_PSTATE_SHIFT_SECOND        (0)

 998 #define MPI2_IOUNITPAGE7_PSTATE_NOT_PRESENT         (0x00)
 999 #define MPI2_IOUNITPAGE7_PSTATE_DISABLED            (0x01)
1000 #define MPI2_IOUNITPAGE7_PSTATE_ENABLED             (0x02)

1002 /* defines for IO Unit Page 7 PowerManagementCapabilities field */
1003 #define MPI25_IOUNITPAGE7_PMCAP_DPA_FULL_PWR_MODE       (0x00400000)
1004 #define MPI25_IOUNITPAGE7_PMCAP_DPA_REDUCED_PWR_MODE    (0x00200000)
```



```
1005 #define MPI25_IOUNITPAGE7_PMCAP_DPA_STANDBY_MODE        (0x00100000)
1006 #define MPI25_IOUNITPAGE7_PMCAP_HOST_FULL_PWR_MODE      (0x00040000)
1007 #define MPI25_IOUNITPAGE7_PMCAP_HOST_REDUCED_PWR_MODE   (0x00020000)
1008 #define MPI25_IOUNITPAGE7_PMCAP_HOST_STANDBY_MODE       (0x00010000)
1009 #define MPI25_IOUNITPAGE7_PMCAP_IO_FULL_PWR_MODE        (0x00004000)
1010 #define MPI25_IOUNITPAGE7_PMCAP_IO_REDUCED_PWR_MODE     (0x00002000)
1011 #define MPI25_IOUNITPAGE7_PMCAP_IO_STANDBY_MODE         (0x00001000)
1012 #define MPI2_IOUNITPAGE7_PMCAP_HOST_12_5_PCT_IOCSPEED   (0x00000400)
1013 #define MPI2_IOUNITPAGE7_PMCAP_HOST_25_0_PCT_IOCSPEED   (0x00000200)
1014 #define MPI2_IOUNITPAGE7_PMCAP_HOST_50_0_PCT_IOCSPEED   (0x00000100)
1015 #define MPI25_IOUNITPAGE7_PMCAP_IO_12_5_PCT_IOCSPEED    (0x00000040)
1016 #define MPI25_IOUNITPAGE7_PMCAP_IO_25_0_PCT_IOCSPEED    (0x00000020)
1017 #define MPI25_IOUNITPAGE7_PMCAP_IO_50_0_PCT_IOCSPEED    (0x00000010)
1018 #define MPI2_IOUNITPAGE7_PMCAP_HOST_WIDTH_CHANGE_PCIE   (0x00000008) /* obsolete
1019 #define MPI2_IOUNITPAGE7_PMCAP_HOST_SPEED_CHANGE_PCIE   (0x00000004) /* obsolete
1020 #define MPI25_IOUNITPAGE7_PMCAP_IO_WIDTH_CHANGE_PCIE    (0x00000002) /* obsolete
1021 #define MPI25_IOUNITPAGE7_PMCAP_IO_SPEED_CHANGE_PCIE    (0x00000001) /* obsolete

1023 /* obsolete names for the PowerManagementCapabilities bits (above) */
1024 #define MPI2_IOUNITPAGE7_PMCAP_12_5_PCT_IOCSPEED    (0x00000400)
1025 #define MPI2_IOUNITPAGE7_PMCAP_25_0_PCT_IOCSPEED    (0x00000200)
1026 #define MPI2_IOUNITPAGE7_PMCAP_50_0_PCT_IOCSPEED    (0x00000100)
1027 #define MPI2_IOUNITPAGE7_PMCAP_PCIE_WIDTH_CHANGE    (0x00000008) /* obsolete */
1028 #define MPI2_IOUNITPAGE7_PMCAP_PCIE_SPEED_CHANGE    (0x00000004) /* obsolete */


1031 /* defines for IO Unit Page 7 IOCTemperatureUnits field */
1032 #define MPI2_IOUNITPAGE7_IOC_TEMP_NOT_PRESENT       (0x00)
1033 #define MPI2_IOUNITPAGE7_IOC_TEMP_FAHRENHEIT        (0x01)
1034 #define MPI2_IOUNITPAGE7_IOC_TEMP_CELSIUS           (0x02)

1036 /* defines for IO Unit Page 7 IOCSpeed field */
1037 #define MPI2_IOUNITPAGE7_IOC_SPEED_FULL             (0x01)
1038 #define MPI2_IOUNITPAGE7_IOC_SPEED_HALF             (0x02)
1039 #define MPI2_IOUNITPAGE7_IOC_SPEED_QUARTER          (0x04)
1040 #define MPI2_IOUNITPAGE7_IOC_SPEED_EIGHTH           (0x08)

1042 /* defines for IO Unit Page 7 BoardTemperatureUnits field */
1043 #define MPI2_IOUNITPAGE7_BOARD_TEMP_NOT_PRESENT     (0x00)
1044 #define MPI2_IOUNITPAGE7_BOARD_TEMP_FAHRENHEIT      (0x01)
1045 #define MPI2_IOUNITPAGE7_BOARD_TEMP_CELSIUS         (0x02)


1048 /* IO Unit Page 8 */

1050 #define MPI2_IOUNIT8_NUM_THRESHOLDS     (4)

1052 typedef struct _MPI2_IOUNIT8_SENSOR
1053 {
1054     U16                     Flags;                              /* 0x00 */
1055     U16                     Reserved1;                          /* 0x02 */
1056     U16                     Threshold[MPI2_IOUNIT8_NUM_THRESHOLDS]; /* 0x04 */
1057     U32                     Reserved2;                          /* 0x0C */
1058     U32                     Reserved3;                          /* 0x10 */
1059     U32                     Reserved4;                          /* 0x14 */
1060 } MPI2_IOUNIT8_SENSOR, MPI2_POINTER PTR_MPI2_IOUNIT8_SENSOR,
1061   Mpi2IOUnit8Sensor_t, MPI2_POINTER pMpi2IOUnit8Sensor_t;

1063 /* defines for IO Unit Page 8 Sensor Flags field */
1064 #define MPI2_IOUNIT8_SENSOR_FLAGS_T3_ENABLE         (0x0008)
1065 #define MPI2_IOUNIT8_SENSOR_FLAGS_T2_ENABLE         (0x0004)
1066 #define MPI2_IOUNIT8_SENSOR_FLAGS_T1_ENABLE         (0x0002)
1067 #define MPI2_IOUNIT8_SENSOR_FLAGS_T0_ENABLE         (0x0001)

1069 /*
1070  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
```

```
 * one and check the value returned for NumSensors at runtime.
 */
#ifndef MPI2_IOUNITPAGE8_SENSOR_ENTRIES
#define MPI2_IOUNITPAGE8_SENSOR_ENTRIES     (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_8
{
    MPI2_CONFIG_PAGE_HEADER Header;                             /* 0x00 */
    U32                     Reserved1;                          /* 0x04 */
    U32                     Reserved2;                          /* 0x08 */
    U8                      NumSensors;                         /* 0x0C */
    U8                      PollingInterval;                    /* 0x0D */
    U16                     Reserved3;                          /* 0x0E */
    MPI2_IOUNIT8_SENSOR     Sensor[MPI2_IOUNITPAGE8_SENSOR_ENTRIES];/* 0x10 */
} MPI2_CONFIG_PAGE_IO_UNIT_8, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_8,
  Mpi2IOUnitPage8_t, MPI2_POINTER pMpi2IOUnitPage8_t;

#define MPI2_IOUNITPAGE8_PAGEVERSION                    (0x00)


/* IO Unit Page 9 */

typedef struct _MPI2_IOUNIT9_SENSOR
{
    U16                     CurrentTemperature;                 /* 0x00 */
    U16                     Reserved1;                          /* 0x02 */
    U8                      Flags;                              /* 0x04 */
    U8                      Reserved2;                          /* 0x05 */
    U16                     Reserved3;                          /* 0x06 */
    U32                     Reserved4;                          /* 0x08 */
    U32                     Reserved5;                          /* 0x0C */
} MPI2_IOUNIT9_SENSOR, MPI2_POINTER PTR_MPI2_IOUNIT9_SENSOR,
  Mpi2IOUnit9Sensor_t, MPI2_POINTER pMpi2IOUnit9Sensor_t;

/* defines for IO Unit Page 9 Sensor Flags field */
#define MPI2_IOUNIT9_SENSOR_FLAGS_TEMP_VALID        (0x01)

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumSensors at runtime.
 */
#ifndef MPI2_IOUNITPAGE9_SENSOR_ENTRIES
#define MPI2_IOUNITPAGE9_SENSOR_ENTRIES     (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_9
{
    MPI2_CONFIG_PAGE_HEADER Header;                             /* 0x00 */
    U32                     Reserved1;                          /* 0x04 */
    U32                     Reserved2;                          /* 0x08 */
    U8                      NumSensors;                         /* 0x0C */
    U8                      Reserved4;                          /* 0x0D */
    U16                     Reserved3;                          /* 0x0E */
    MPI2_IOUNIT9_SENSOR     Sensor[MPI2_IOUNITPAGE9_SENSOR_ENTRIES];/* 0x10 */
} MPI2_CONFIG_PAGE_IO_UNIT_9, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_9,
  Mpi2IOUnitPage9_t, MPI2_POINTER pMpi2IOUnitPage9_t;

#define MPI2_IOUNITPAGE9_PAGEVERSION                    (0x00)


/* IO Unit Page 10 */

typedef struct _MPI2_IOUNIT10_FUNCTION
{
    U8                      CreditPercent;      /* 0x00 */
```



```
    U8                      Reserved1;          /* 0x01 */
    U16                     Reserved2;          /* 0x02 */
} MPI2_IOUNIT10_FUNCTION, MPI2_POINTER PTR_MPI2_IOUNIT10_FUNCTION,
  Mpi2IOUnit10Function_t, MPI2_POINTER pMpi2IOUnit10Function_t;

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumFunctions at runtime.
 */
#ifndef MPI2_IOUNITPAGE10_FUNCTION_ENTRIES
#define MPI2_IOUNITPAGE10_FUNCTION_ENTRIES      (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_IO_UNIT_10
{
    MPI2_CONFIG_PAGE_HEADER Header;                                     /* 0
    U8                      NumFunctions;                               /* 0
    U8                      Reserved1;                                  /* 0
    U16                     Reserved2;                                  /* 0
    U32                     Reserved3;                                  /* 0
    U32                     Reserved4;                                  /* 0
    MPI2_IOUNIT10_FUNCTION  Function[MPI2_IOUNITPAGE10_FUNCTION_ENTRIES];   /* 0
} MPI2_CONFIG_PAGE_IO_UNIT_10, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IO_UNIT_10,
  Mpi2IOUnitPage10_t, MPI2_POINTER pMpi2IOUnitPage10_t;

#define MPI2_IOUNITPAGE10_PAGEVERSION                   (0x01)




/*****************************************************************************
*   IOC Config Pages
*****************************************************************************/

/* IOC Page 0 */

typedef struct _MPI2_CONFIG_PAGE_IOC_0
{
    MPI2_CONFIG_PAGE_HEADER Header;                     /* 0x00 */
    U32                     Reserved1;                  /* 0x04 */
    U32                     Reserved2;                  /* 0x08 */
    U16                     VendorID;                   /* 0x0C */
    U16                     DeviceID;                   /* 0x0E */
    U8                      RevisionID;                 /* 0x10 */
    U8                      Reserved3;                  /* 0x11 */
    U16                     Reserved4;                  /* 0x12 */
    U32                     ClassCode;                  /* 0x14 */
    U16                     SubsystemVendorID;          /* 0x18 */
    U16                     SubsystemID;                /* 0x1A */
} MPI2_CONFIG_PAGE_IOC_0, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IOC_0,
_____unchanged_portion_omitted_
  Mpi2IOCPage6_t, MPI2_POINTER pMpi2IOCPage6_t;

#define MPI2_IOCPAGE6_PAGEVERSION                       (0x05)
 997 #define MPI2_IOCPAGE6_PAGEVERSION                  (0x04)

/* defines for IOC Page 6 CapabilitiesFlags */
#define MPI2_IOCPAGE6_CAP_FLAGS_4K_SECTORS_SUPPORT      (0x00000020)
#define MPI2_IOCPAGE6_CAP_FLAGS_RAID10_SUPPORT          (0x00000010)
#define MPI2_IOCPAGE6_CAP_FLAGS_RAID1_SUPPORT           (0x00000008)
#define MPI2_IOCPAGE6_CAP_FLAGS_RAID1E_SUPPORT          (0x00000004)
#define MPI2_IOCPAGE6_CAP_FLAGS_RAID0_SUPPORT           (0x00000002)
#define MPI2_IOCPAGE6_CAP_FLAGS_GLOBAL_HOT_SPARE        (0x00000001)


/* IOC Page 7 */
```

```
#define MPI2_IOCPAGE7_EVENTMASK_WORDS       (4)

typedef struct _MPI2_CONFIG_PAGE_IOC_7
{
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x00 */
    U32                     Reserved1;              /* 0x04 */
    U32                     EventMasks[MPI2_IOCPAGE7_EVENTMASK_WORDS];/* 0x08 */
    U16                     SASBroadcastPrimitiveMasks; /* 0x18 */
    U16                     SASNotifyPrimitiveMasks;    /* 0x1A */
    U16                     Reserved2;              /* 0x1A */
    U32                     Reserved3;              /* 0x1C */
} MPI2_CONFIG_PAGE_IOC_7, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IOC_7,
  Mpi2IOCPage7_t, MPI2_POINTER pMpi2IOCPage7_t;

#define MPI2_IOCPAGE7_PAGEVERSION                   (0x02)
#define MPI2_IOCPAGE7_PAGEVERSION                   (0x01)


/* IOC Page 8 */

typedef struct _MPI2_CONFIG_PAGE_IOC_8
{
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x00 */
    U8                      NumDevsPerEnclosure;    /* 0x04 */
    U8                      Reserved1;              /* 0x05 */
    U16                     Reserved2;              /* 0x06 */
    U16                     MaxPersistentEntries;   /* 0x08 */
    U16                     MaxNumPhysicalMappedIDs;/* 0x0A */
    U16                     Flags;                  /* 0x0C */
    U16                     Reserved3;              /* 0x0E */
    U16                     IRVolumeMappingFlags;   /* 0x10 */
    U16                     Reserved4;              /* 0x12 */
    U32                     Reserved5;              /* 0x14 */
} MPI2_CONFIG_PAGE_IOC_8, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_IOC_8,
  Mpi2IOCPage8_t, MPI2_POINTER pMpi2IOCPage8_t;

#define MPI2_IOCPAGE8_PAGEVERSION                   (0x00)

/* defines for IOC Page 8 Flags field */
#define MPI2_IOCPAGE8_FLAGS_DA_START_SLOT_1         (0x00000020)
#define MPI2_IOCPAGE8_FLAGS_RESERVED_TARGETID_0     (0x00000010)

#define MPI2_IOCPAGE8_FLAGS_MASK_MAPPING_MODE       (0x0000000E)
#define MPI2_IOCPAGE8_FLAGS_DEVICE_PERSISTENCE_MAPPING  (0x00000000)
#define MPI2_IOCPAGE8_FLAGS_ENCLOSURE_SLOT_MAPPING  (0x00000002)

#define MPI2_IOCPAGE8_FLAGS_DISABLE_PERSISTENT_MAPPING  (0x00000001)
#define MPI2_IOCPAGE8_FLAGS_ENABLE_PERSISTENT_MAPPING   (0x00000000)

/* defines for IOC Page 8 IRVolumeMappingFlags */
#define MPI2_IOCPAGE8_IRFLAGS_MASK_VOLUME_MAPPING_MODE  (0x00000003)
#define MPI2_IOCPAGE8_IRFLAGS_LOW_VOLUME_MAPPING    (0x00000000)
#define MPI2_IOCPAGE8_IRFLAGS_HIGH_VOLUME_MAPPING   (0x00000001)


/*****************************************************************************
*   BIOS Config Pages
*****************************************************************************/

/* BIOS Page 1 */

typedef struct _MPI2_CONFIG_PAGE_BIOS_1
{
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x00 */
    U32                     BiosOptions;            /* 0x04 */
    U32                     IOCSettings;            /* 0x08 */
```



```
    U32                     Reserved1;              /* 0x0C */
    U32                     DeviceSettings;         /* 0x10 */
    U16                     NumberOfDevices;        /* 0x14 */
    U16                     UEFIVersion;            /* 0x16 */
    U16                     Reserved2;              /* 0x16 */
    U16                     IOTimeoutBlockDevicesNonRM; /* 0x18 */
    U16                     IOTimeoutSequential;    /* 0x1A */
    U16                     IOTimeoutOther;         /* 0x1C */
    U16                     IOTimeoutBlockDevicesRM;    /* 0x1E */
} MPI2_CONFIG_PAGE_BIOS_1, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_BIOS_1,
  Mpi2BiosPage1_t, MPI2_POINTER pMpi2BiosPage1_t;

#define MPI2_BIOSPAGE1_PAGEVERSION                  (0x05)
#define MPI2_BIOSPAGE1_PAGEVERSION                  (0x04)

/* values for BIOS Page 1 BiosOptions field */
#define MPI2_BIOSPAGE1_OPTIONS_MASK_OEM_ID                  (0x000000F0)
#define MPI2_BIOSPAGE1_OPTIONS_LSI_OEM_ID                   (0x00000000)

#define MPI2_BIOSPAGE1_OPTIONS_MASK_UEFI_HII_REGISTRATION   (0x00000006)
#define MPI2_BIOSPAGE1_OPTIONS_ENABLE_UEFI_HII              (0x00000000)
#define MPI2_BIOSPAGE1_OPTIONS_DISABLE_UEFI_HII             (0x00000002)
#define MPI2_BIOSPAGE1_OPTIONS_VERSION_CHECK_UEFI_HII       (0x00000004)

#define MPI2_BIOSPAGE1_OPTIONS_DISABLE_BIOS                 (0x00000001)

/* values for BIOS Page 1 IOCSettings field */
#define MPI2_BIOSPAGE1_IOCSET_MASK_BOOT_PREFERENCE      (0x00030000)
#define MPI2_BIOSPAGE1_IOCSET_ENCLOSURE_SLOT_BOOT       (0x00000000)
#define MPI2_BIOSPAGE1_IOCSET_SAS_ADDRESS_BOOT          (0x00010000)

#define MPI2_BIOSPAGE1_IOCSET_MASK_RM_SETTING           (0x000000C0)
#define MPI2_BIOSPAGE1_IOCSET_NONE_RM_SETTING           (0x00000000)
#define MPI2_BIOSPAGE1_IOCSET_BOOT_RM_SETTING           (0x00000040)
#define MPI2_BIOSPAGE1_IOCSET_MEDIA_RM_SETTING          (0x00000080)

#define MPI2_BIOSPAGE1_IOCSET_MASK_ADAPTER_SUPPORT      (0x00000030)
#define MPI2_BIOSPAGE1_IOCSET_NO_SUPPORT                (0x00000000)
#define MPI2_BIOSPAGE1_IOCSET_BIOS_SUPPORT              (0x00000010)
#define MPI2_BIOSPAGE1_IOCSET_OS_SUPPORT                (0x00000020)
#define MPI2_BIOSPAGE1_IOCSET_ALL_SUPPORT               (0x00000030)

#define MPI2_BIOSPAGE1_IOCSET_ALTERNATE_CHS             (0x00000008)

/* values for BIOS Page 1 DeviceSettings field */
#define MPI2_BIOSPAGE1_DEVSET_DISABLE_SMART_POLLING     (0x00000010)
#define MPI2_BIOSPAGE1_DEVSET_DISABLE_SEQ_LUN           (0x00000008)
#define MPI2_BIOSPAGE1_DEVSET_DISABLE_RM_LUN            (0x00000004)
#define MPI2_BIOSPAGE1_DEVSET_DISABLE_NON_RM_LUN        (0x00000002)
#define MPI2_BIOSPAGE1_DEVSET_DISABLE_OTHER_LUN         (0x00000001)

/* defines for BIOS Page 1 UEFIVersion field */
#define MPI2_BIOSPAGE1_UEFI_VER_MAJOR_MASK              (0xFF00)
#define MPI2_BIOSPAGE1_UEFI_VER_MAJOR_SHIFT             (8)
#define MPI2_BIOSPAGE1_UEFI_VER_MINOR_MASK              (0x00FF)
#define MPI2_BIOSPAGE1_UEFI_VER_MINOR_SHIFT             (0)


/* BIOS Page 2 */

typedef struct _MPI2_BOOT_DEVICE_ADAPTER_ORDER
{
    U32         Reserved1;                          /* 0x00 */
    U32         Reserved2;                          /* 0x04 */
    U32         Reserved3;                          /* 0x08 */
```

```
1392     U32         Reserved4;                              /* 0x0C */
1393     U32         Reserved5;                              /* 0x10 */
1394     U32         Reserved6;                              /* 0x14 */
1395 } MPI2_BOOT_DEVICE_ADAPTER_ORDER,
_____unchanged_portion_omitted_
1493   Mpi2BiosPage3_t, MPI2_POINTER pMpi2BiosPage3_t;

1495 #define MPI2_BIOSPAGE3_PAGEVERSION                      (0x00)

1497 /* values for BIOS Page 3 GlobalFlags */
1498 #define MPI2_BIOSPAGE3_FLAGS_PAUSE_ON_ERROR             (0x00000002)
1499 #define MPI2_BIOSPAGE3_FLAGS_VERBOSE_ENABLE             (0x00000004)
1500 #define MPI2_BIOSPAGE3_FLAGS_HOOK_INT_40_DISABLE        (0x00000010)

1502 #define MPI2_BIOSPAGE3_FLAGS_DEV_LIST_DISPLAY_MASK      (0x000000E0)
1503 #define MPI2_BIOSPAGE3_FLAGS_INSTALLED_DEV_DISPLAY      (0x00000000)
1504 #define MPI2_BIOSPAGE3_FLAGS_ADAPTER_DISPLAY            (0x00000020)
1505 #define MPI2_BIOSPAGE3_FLAGS_ADAPTER_DEV_DISPLAY        (0x00000040)


1508 /* BIOS Page 4 */

1510 /*
1511  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
1512  * one and check the value returned for NumPhys at runtime.
1242  * one and check Header.PageLength or NumPhys at runtime.
1513  */
1514 #ifndef MPI2_BIOS_PAGE_4_PHY_ENTRIES
1515 #define MPI2_BIOS_PAGE_4_PHY_ENTRIES        (1)
1516 #endif

1518 typedef struct _MPI2_BIOS4_ENTRY
1519 {
1520     U64                     ReassignmentWWID;       /* 0x00 */
1521     U64                     ReassignmentDeviceName; /* 0x08 */
1522 } MPI2_BIOS4_ENTRY, MPI2_POINTER PTR_MPI2_BIOS4_ENTRY,
_____unchanged_portion_omitted_
1563   Mpi2RaidVol0Settings_t, MPI2_POINTER pMpi2RaidVol0Settings_t;

1565 /* RAID Volume Page 0 HotSparePool defines, also used in RAID Physical Disk */
1566 #define MPI2_RAID_HOT_SPARE_POOL_0                      (0x01)
1567 #define MPI2_RAID_HOT_SPARE_POOL_1                      (0x02)
1568 #define MPI2_RAID_HOT_SPARE_POOL_2                      (0x04)
1569 #define MPI2_RAID_HOT_SPARE_POOL_3                      (0x08)
1570 #define MPI2_RAID_HOT_SPARE_POOL_4                      (0x10)
1571 #define MPI2_RAID_HOT_SPARE_POOL_5                      (0x20)
1572 #define MPI2_RAID_HOT_SPARE_POOL_6                      (0x40)
1573 #define MPI2_RAID_HOT_SPARE_POOL_7                      (0x80)

1575 /* RAID Volume Page 0 VolumeSettings defines */
1576 #define MPI2_RAIDVOL0_SETTING_USE_PRODUCT_ID_SUFFIX     (0x0008)
1577 #define MPI2_RAIDVOL0_SETTING_AUTO_CONFIG_HSWAP_DISABLE (0x0004)

1579 #define MPI2_RAIDVOL0_SETTING_MASK_WRITE_CACHING        (0x0003)
1580 #define MPI2_RAIDVOL0_SETTING_UNCHANGED                 (0x0000)
1581 #define MPI2_RAIDVOL0_SETTING_DISABLE_WRITE_CACHING     (0x0001)
1582 #define MPI2_RAIDVOL0_SETTING_ENABLE_WRITE_CACHING      (0x0002)

1584 /*
1585  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
1586  * one and check the value returned for NumPhysDisks at runtime.
1316  * one and check Header.PageLength at runtime.
1587  */
1588 #ifndef MPI2_RAID_VOL_PAGE_0_PHYSDISK_MAX
1589 #define MPI2_RAID_VOL_PAGE_0_PHYSDISK_MAX       (1)
1590 #endif
```



```
1592 typedef struct _MPI2_CONFIG_PAGE_RAID_VOL_0
1593 {
1594     MPI2_CONFIG_PAGE_HEADER Header;                     /* 0x00 */
1595     U16                     DevHandle;                  /* 0x04 */
1596     U8                      VolumeState;                /* 0x06 */
1597     U8                      VolumeType;                 /* 0x07 */
1598     U32                     VolumeStatusFlags;          /* 0x08 */
1599     MPI2_RAIDVOL0_SETTINGS  VolumeSettings;             /* 0x0C */
1600     U64                     MaxLBA;                     /* 0x10 */
1601     U32                     StripeSize;                 /* 0x18 */
1602     U16                     BlockSize;                  /* 0x1C */
1603     U16                     Reserved1;                  /* 0x1E */
1604     U8                      SupportedPhysDisks;         /* 0x20 */
1605     U8                      ResyncRate;                 /* 0x21 */
1606     U16                     DataScrubDuration;          /* 0x22 */
1607     U8                      NumPhysDisks;               /* 0x24 */
1608     U8                      Reserved2;                  /* 0x25 */
1609     U8                      Reserved3;                  /* 0x26 */
1610     U8                      InactiveStatus;             /* 0x27 */
1611     MPI2_RAIDVOL0_PHYS_DISK PhysDisk[MPI2_RAID_VOL_PAGE_0_PHYSDISK_MAX]; /* 0x28
1612 } MPI2_CONFIG_PAGE_RAID_VOL_0, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_RAID_VOL_0,
1613   Mpi2RaidVolPage0_t, MPI2_POINTER pMpi2RaidVolPage0_t;

1615 #define MPI2_RAIDVOLPAGE0_PAGEVERSION           (0x0A)

1617 /* values for RAID VolumeState */
1618 #define MPI2_RAID_VOL_STATE_MISSING                         (0x00)
1619 #define MPI2_RAID_VOL_STATE_FAILED                          (0x01)
1620 #define MPI2_RAID_VOL_STATE_INITIALIZING                    (0x02)
1621 #define MPI2_RAID_VOL_STATE_ONLINE                          (0x03)
1622 #define MPI2_RAID_VOL_STATE_DEGRADED                        (0x04)
1623 #define MPI2_RAID_VOL_STATE_OPTIMAL                         (0x05)

1625 /* values for RAID VolumeType */
1626 #define MPI2_RAID_VOL_TYPE_RAID0                            (0x00)
1627 #define MPI2_RAID_VOL_TYPE_RAID1E                           (0x01)
1628 #define MPI2_RAID_VOL_TYPE_RAID1                            (0x02)
1629 #define MPI2_RAID_VOL_TYPE_RAID10                           (0x05)
1630 #define MPI2_RAID_VOL_TYPE_UNKNOWN                          (0xFF)

1632 /* values for RAID Volume Page 0 VolumeStatusFlags field */
1633 #define MPI2_RAIDVOL0_STATUS_FLAG_PENDING_RESYNC            (0x02000000)
1634 #define MPI2_RAIDVOL0_STATUS_FLAG_BACKG_INIT_PENDING        (0x01000000)
1635 #define MPI2_RAIDVOL0_STATUS_FLAG_MDC_PENDING               (0x00800000)
1636 #define MPI2_RAIDVOL0_STATUS_FLAG_USER_CONSIST_PENDING      (0x00400000)
1637 #define MPI2_RAIDVOL0_STATUS_FLAG_MAKE_DATA_CONSISTENT      (0x00200000)
1638 #define MPI2_RAIDVOL0_STATUS_FLAG_DATA_SCRUB                (0x00100000)
1639 #define MPI2_RAIDVOL0_STATUS_FLAG_CONSISTENCY_CHECK         (0x00080000)
1640 #define MPI2_RAIDVOL0_STATUS_FLAG_CAPACITY_EXPANSION        (0x00040000)
1641 #define MPI2_RAIDVOL0_STATUS_FLAG_BACKGROUND_INIT           (0x00020000)
1642 #define MPI2_RAIDVOL0_STATUS_FLAG_RESYNC_IN_PROGRESS        (0x00010000)
1643 #define MPI2_RAIDVOL0_STATUS_FLAG_VOL_NOT_CONSISTENT        (0x00000080)
1644 #define MPI2_RAIDVOL0_STATUS_FLAG_OCE_ALLOWED               (0x00000040)
1645 #define MPI2_RAIDVOL0_STATUS_FLAG_BGI_COMPLETE              (0x00000020)
1646 #define MPI2_RAIDVOL0_STATUS_FLAG_1E_OFFSET_MIRROR          (0x00000000)
1647 #define MPI2_RAIDVOL0_STATUS_FLAG_1E_ADJACENT_MIRROR        (0x00000010)
1648 #define MPI2_RAIDVOL0_STATUS_FLAG_BAD_BLOCK_TABLE_FULL      (0x00000008)
1649 #define MPI2_RAIDVOL0_STATUS_FLAG_VOLUME_INACTIVE           (0x00000004)
1650 #define MPI2_RAIDVOL0_STATUS_FLAG_QUIESCED                  (0x00000002)
1651 #define MPI2_RAIDVOL0_STATUS_FLAG_ENABLED                   (0x00000001)

1653 /* values for RAID Volume Page 0 SupportedPhysDisks field */
1654 #define MPI2_RAIDVOL0_SUPPORT_SOLID_STATE_DISKS             (0x08)
1655 #define MPI2_RAIDVOL0_SUPPORT_HARD_DISKS                    (0x04)
1656 #define MPI2_RAIDVOL0_SUPPORT_SAS_PROTOCOL                  (0x02)
```

```
#define MPI2_RAIDVOL0_SUPPORT_SATA_PROTOCOL                (0x01)

/* values for RAID Volume Page 0 InactiveStatus field */
#define MPI2_RAIDVOLPAGE0_UNKNOWN_INACTIVE                 (0x00)
#define MPI2_RAIDVOLPAGE0_STALE_METADATA_INACTIVE          (0x01)
#define MPI2_RAIDVOLPAGE0_FOREIGN_VOLUME_INACTIVE          (0x02)
#define MPI2_RAIDVOLPAGE0_INSUFFICIENT_RESOURCE_INACTIVE   (0x03)
#define MPI2_RAIDVOLPAGE0_CLONE_VOLUME_INACTIVE            (0x04)
#define MPI2_RAIDVOLPAGE0_INSUFFICIENT_METADATA_INACTIVE   (0x05)
#define MPI2_RAIDVOLPAGE0_PREVIOUSLY_DELETED               (0x06)


/* RAID Volume Page 1 */

typedef struct _MPI2_CONFIG_PAGE_RAID_VOL_1
{
    MPI2_CONFIG_PAGE_HEADER Header;                 /* 0x00 */
    U16                     DevHandle;              /* 0x04 */
    U16                     Reserved0;              /* 0x06 */
    U8                      GUID[24];               /* 0x08 */
    U8                      Name[16];               /* 0x20 */
    U64                     WWID;                   /* 0x30 */
    U32                     Reserved1;              /* 0x38 */
    U32                     Reserved2;              /* 0x3C */
} MPI2_CONFIG_PAGE_RAID_VOL_1, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_RAID_VOL_1,
_____unchanged_portion_omitted_
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_RD_PDISK_0,
  Mpi2RaidPhysDiskPage0_t, MPI2_POINTER pMpi2RaidPhysDiskPage0_t;

#define MPI2_RAIDPHYSDISKPAGE0_PAGEVERSION          (0x05)

/* PhysDiskState defines */
#define MPI2_RAID_PD_STATE_NOT_CONFIGURED               (0x00)
#define MPI2_RAID_PD_STATE_NOT_COMPATIBLE               (0x01)
#define MPI2_RAID_PD_STATE_OFFLINE                      (0x02)
#define MPI2_RAID_PD_STATE_ONLINE                       (0x03)
#define MPI2_RAID_PD_STATE_HOT_SPARE                    (0x04)
#define MPI2_RAID_PD_STATE_DEGRADED                     (0x05)
#define MPI2_RAID_PD_STATE_REBUILDING                   (0x06)
#define MPI2_RAID_PD_STATE_OPTIMAL                      (0x07)

/* OfflineReason defines */
#define MPI2_PHYSDISK0_ONLINE                           (0x00)
#define MPI2_PHYSDISK0_OFFLINE_MISSING                  (0x01)
#define MPI2_PHYSDISK0_OFFLINE_FAILED                   (0x03)
#define MPI2_PHYSDISK0_OFFLINE_INITIALIZING             (0x04)
#define MPI2_PHYSDISK0_OFFLINE_REQUESTED                (0x05)
#define MPI2_PHYSDISK0_OFFLINE_FAILED_REQUESTED         (0x06)
#define MPI2_PHYSDISK0_OFFLINE_OTHER                    (0xFF)

/* IncompatibleReason defines */
#define MPI2_PHYSDISK0_COMPATIBLE                       (0x00)
#define MPI2_PHYSDISK0_INCOMPATIBLE_PROTOCOL            (0x01)
#define MPI2_PHYSDISK0_INCOMPATIBLE_BLOCKSIZE           (0x02)
#define MPI2_PHYSDISK0_INCOMPATIBLE_MAX_LBA             (0x03)
#define MPI2_PHYSDISK0_INCOMPATIBLE_SATA_EXTENDED_CMD   (0x04)
#define MPI2_PHYSDISK0_INCOMPATIBLE_REMOVEABLE_MEDIA    (0x05)
#define MPI2_PHYSDISK0_INCOMPATIBLE_MEDIA_TYPE          (0x06)
#define MPI2_PHYSDISK0_INCOMPATIBLE_UNKNOWN             (0xFF)

/* PhysDiskAttributes defines */
#define MPI2_PHYSDISK0_ATTRIB_MEDIA_MASK                (0x0C)
#define MPI2_PHYSDISK0_ATTRIB_SOLID_STATE_DRIVE         (0x08)
#define MPI2_PHYSDISK0_ATTRIB_HARD_DISK_DRIVE           (0x04)

#define MPI2_PHYSDISK0_ATTRIB_PROTOCOL_MASK             (0x03)
```



```
#define MPI2_PHYSDISK0_ATTRIB_SAS_PROTOCOL              (0x02)
#define MPI2_PHYSDISK0_ATTRIB_SATA_PROTOCOL             (0x01)

/* PhysDiskStatusFlags defines */
#define MPI2_PHYSDISK0_STATUS_FLAG_NOT_CERTIFIED        (0x00000040)
#define MPI2_PHYSDISK0_STATUS_FLAG_OCE_TARGET           (0x00000020)
#define MPI2_PHYSDISK0_STATUS_FLAG_WRITE_CACHE_ENABLED  (0x00000010)
#define MPI2_PHYSDISK0_STATUS_FLAG_OPTIMAL_PREVIOUS     (0x00000000)
#define MPI2_PHYSDISK0_STATUS_FLAG_NOT_OPTIMAL_PREVIOUS (0x00000008)
#define MPI2_PHYSDISK0_STATUS_FLAG_INACTIVE_VOLUME      (0x00000004)
#define MPI2_PHYSDISK0_STATUS_FLAG_QUIESCED             (0x00000002)
#define MPI2_PHYSDISK0_STATUS_FLAG_OUT_OF_SYNC          (0x00000001)


/* RAID Physical Disk Page 1 */

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumPhysDiskPaths at runtime.
 * one and check Header.PageLength or NumPhysDiskPaths at runtime.
 */
#ifndef MPI2_RAID_PHYS_DISK1_PATH_MAX
#define MPI2_RAID_PHYS_DISK1_PATH_MAX   (1)
#endif

typedef struct _MPI2_RAIDPHYSDISK1_PATH
{
    U16             DevHandle;          /* 0x00 */
    U16             Reserved1;          /* 0x02 */
    U64             WWID;               /* 0x04 */
    U64             OwnerWWID;          /* 0x0C */
    U8              OwnerIdentifier;    /* 0x14 */
    U8              Reserved2;          /* 0x15 */
    U16             Flags;              /* 0x16 */
} MPI2_RAIDPHYSDISK1_PATH, MPI2_POINTER PTR_MPI2_RAIDPHYSDISK1_PATH,
_____unchanged_portion_omitted_
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_RD_PDISK_1,
  Mpi2RaidPhysDiskPage1_t, MPI2_POINTER pMpi2RaidPhysDiskPage1_t;

#define MPI2_RAIDPHYSDISKPAGE1_PAGEVERSION          (0x02)


/*******************************************************************************
*   values for fields used by several types of SAS Config Pages
*******************************************************************************/

/* values for NegotiatedLinkRates fields */
#define MPI2_SAS_NEG_LINK_RATE_MASK_LOGICAL             (0xF0)
#define MPI2_SAS_NEG_LINK_RATE_SHIFT_LOGICAL            (4)
#define MPI2_SAS_NEG_LINK_RATE_MASK_PHYSICAL            (0x0F)
/* link rates used for Negotiated Physical and Logical Link Rate */
#define MPI2_SAS_NEG_LINK_RATE_UNKNOWN_LINK_RATE        (0x00)
#define MPI2_SAS_NEG_LINK_RATE_PHY_DISABLED             (0x01)
#define MPI2_SAS_NEG_LINK_RATE_NEGOTIATION_FAILED       (0x02)
#define MPI2_SAS_NEG_LINK_RATE_SATA_OOB_COMPLETE        (0x03)
#define MPI2_SAS_NEG_LINK_RATE_PORT_SELECTOR            (0x04)
#define MPI2_SAS_NEG_LINK_RATE_SMP_RESET_IN_PROGRESS    (0x05)
#define MPI2_SAS_NEG_LINK_RATE_UNSUPPORTED_PHY          (0x06)
#define MPI2_SAS_NEG_LINK_RATE_1_5                      (0x08)
#define MPI2_SAS_NEG_LINK_RATE_3_0                      (0x09)
#define MPI2_SAS_NEG_LINK_RATE_6_0                      (0x0A)
#define MPI25_SAS_NEG_LINK_RATE_12_0                    (0x0B)


/* values for AttachedPhyInfo fields */
#define MPI2_SAS_APHYINFO_INSIDE_ZPSDS_PERSISTENT       (0x00000040)
```

```
#define MPI2_SAS_APHYINFO_REQUESTED_INSIDE_ZPSDS        (0x00000020)
#define MPI2_SAS_APHYINFO_BREAK_REPLY_CAPABLE           (0x00000010)

#define MPI2_SAS_APHYINFO_REASON_MASK                   (0x0000000F)
#define MPI2_SAS_APHYINFO_REASON_UNKNOWN                (0x00000000)
#define MPI2_SAS_APHYINFO_REASON_POWER_ON               (0x00000001)
#define MPI2_SAS_APHYINFO_REASON_HARD_RESET             (0x00000002)
#define MPI2_SAS_APHYINFO_REASON_SMP_PHY_CONTROL        (0x00000003)
#define MPI2_SAS_APHYINFO_REASON_LOSS_OF_SYNC           (0x00000004)
#define MPI2_SAS_APHYINFO_REASON_MULTIPLEXING_SEQ       (0x00000005)
#define MPI2_SAS_APHYINFO_REASON_IT_NEXUS_LOSS_TIMER    (0x00000006)
#define MPI2_SAS_APHYINFO_REASON_BREAK_TIMEOUT          (0x00000007)
#define MPI2_SAS_APHYINFO_REASON_PHY_TEST_STOPPED       (0x00000008)


/* values for PhyInfo fields */
#define MPI2_SAS_PHYINFO_PHY_VACANT                     (0x80000000)

#define MPI2_SAS_PHYINFO_PHY_POWER_CONDITION_MASK       (0x18000000)
#define MPI2_SAS_PHYINFO_SHIFT_PHY_POWER_CONDITION      (27)
#define MPI2_SAS_PHYINFO_PHY_POWER_ACTIVE               (0x00000000)
#define MPI2_SAS_PHYINFO_PHY_POWER_PARTIAL              (0x08000000)
#define MPI2_SAS_PHYINFO_PHY_POWER_SLUMBER              (0x10000000)

#define MPI2_SAS_PHYINFO_CHANGED_REQ_INSIDE_ZPSDS       (0x04000000)
#define MPI2_SAS_PHYINFO_INSIDE_ZPSDS_PERSISTENT        (0x02000000)
#define MPI2_SAS_PHYINFO_REQ_INSIDE_ZPSDS               (0x01000000)
#define MPI2_SAS_PHYINFO_ZONE_GROUP_PERSISTENT          (0x00400000)
#define MPI2_SAS_PHYINFO_INSIDE_ZPSDS                   (0x00200000)
#define MPI2_SAS_PHYINFO_ZONING_ENABLED                 (0x00100000)

#define MPI2_SAS_PHYINFO_REASON_MASK                    (0x000F0000)
#define MPI2_SAS_PHYINFO_REASON_UNKNOWN                 (0x00000000)
#define MPI2_SAS_PHYINFO_REASON_POWER_ON                (0x00010000)
#define MPI2_SAS_PHYINFO_REASON_HARD_RESET              (0x00020000)
#define MPI2_SAS_PHYINFO_REASON_SMP_PHY_CONTROL         (0x00030000)
#define MPI2_SAS_PHYINFO_REASON_LOSS_OF_SYNC            (0x00040000)
#define MPI2_SAS_PHYINFO_REASON_MULTIPLEXING_SEQ        (0x00050000)
#define MPI2_SAS_PHYINFO_REASON_IT_NEXUS_LOSS_TIMER     (0x00060000)
#define MPI2_SAS_PHYINFO_REASON_BREAK_TIMEOUT           (0x00070000)
#define MPI2_SAS_PHYINFO_REASON_PHY_TEST_STOPPED        (0x00080000)

#define MPI2_SAS_PHYINFO_MULTIPLEXING_SUPPORTED         (0x00008000)
#define MPI2_SAS_PHYINFO_SATA_PORT_ACTIVE               (0x00004000)
#define MPI2_SAS_PHYINFO_SATA_PORT_SELECTOR_PRESENT     (0x00002000)
#define MPI2_SAS_PHYINFO_VIRTUAL_PHY                    (0x00001000)

#define MPI2_SAS_PHYINFO_MASK_PARTIAL_PATHWAY_TIME      (0x00000F00)
#define MPI2_SAS_PHYINFO_SHIFT_PARTIAL_PATHWAY_TIME     (8)

#define MPI2_SAS_PHYINFO_MASK_ROUTING_ATTRIBUTE         (0x000000F0)
#define MPI2_SAS_PHYINFO_DIRECT_ROUTING                 (0x00000000)
#define MPI2_SAS_PHYINFO_SUBTRACTIVE_ROUTING            (0x00000010)
#define MPI2_SAS_PHYINFO_TABLE_ROUTING                  (0x00000020)


/* values for SAS ProgrammedLinkRate fields */
#define MPI2_SAS_PRATE_MAX_RATE_MASK                    (0xF0)
#define MPI2_SAS_PRATE_MAX_RATE_NOT_PROGRAMMABLE        (0x00)
#define MPI2_SAS_PRATE_MAX_RATE_1_5                     (0x80)
#define MPI2_SAS_PRATE_MAX_RATE_3_0                     (0x90)
#define MPI2_SAS_PRATE_MAX_RATE_6_0                     (0xA0)
#define MPI25_SAS_PRATE_MAX_RATE_12_0                   (0xB0)
#define MPI2_SAS_PRATE_MIN_RATE_MASK                    (0x0F)
#define MPI2_SAS_PRATE_MIN_RATE_NOT_PROGRAMMABLE        (0x00)
#define MPI2_SAS_PRATE_MIN_RATE_1_5                     (0x08)
```



```
#define MPI2_SAS_PRATE_MIN_RATE_3_0                     (0x09)
#define MPI2_SAS_PRATE_MIN_RATE_6_0                     (0x0A)
#define MPI25_SAS_PRATE_MIN_RATE_12_0                   (0x0B)


/* values for SAS HwLinkRate fields */
#define MPI2_SAS_HWRATE_MAX_RATE_MASK                   (0xF0)
#define MPI2_SAS_HWRATE_MAX_RATE_1_5                    (0x80)
#define MPI2_SAS_HWRATE_MAX_RATE_3_0                    (0x90)
#define MPI2_SAS_HWRATE_MAX_RATE_6_0                    (0xA0)
#define MPI25_SAS_HWRATE_MAX_RATE_12_0                  (0xB0)
#define MPI2_SAS_HWRATE_MIN_RATE_MASK                   (0x0F)
#define MPI2_SAS_HWRATE_MIN_RATE_1_5                    (0x08)
#define MPI2_SAS_HWRATE_MIN_RATE_3_0                    (0x09)
#define MPI2_SAS_HWRATE_MIN_RATE_6_0                    (0x0A)
#define MPI25_SAS_HWRATE_MIN_RATE_12_0                  (0x0B)



/****************************************************************************
*   SAS IO Unit Config Pages
****************************************************************************/

/* SAS IO Unit Page 0 */

typedef struct _MPI2_SAS_IO_UNIT0_PHY_DATA
{
    U8          Port;                   /* 0x00 */
    U8          PortFlags;              /* 0x01 */
    U8          PhyFlags;               /* 0x02 */
    U8          NegotiatedLinkRate;     /* 0x03 */
    U32         ControllerPhyDeviceInfo;/* 0x04 */
    U16         AttachedDevHandle;      /* 0x08 */
    U16         ControllerDevHandle;    /* 0x0A */
    U32         DiscoveryStatus;        /* 0x0C */
    U32         Reserved;               /* 0x10 */
} MPI2_SAS_IO_UNIT0_PHY_DATA, MPI2_POINTER PTR_MPI2_SAS_IO_UNIT0_PHY_DATA,
  Mpi2SasIOUnit0PhyData_t, MPI2_POINTER pMpi2SasIOUnit0PhyData_t;

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumPhys at runtime.
 * one and check Header.ExtPageLength or NumPhys at runtime.
 */
#ifndef MPI2_SAS_IOUNIT0_PHY_MAX
#define MPI2_SAS_IOUNIT0_PHY_MAX        (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_0
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                             /* 0
    U32                                 Reserved1;                          /* 0
    U8                                  NumPhys;                            /* 0
    U8                                  Reserved2;                          /* 0
    U16                                 Reserved3;                          /* 0
    MPI2_SAS_IO_UNIT0_PHY_DATA          PhyData[MPI2_SAS_IOUNIT0_PHY_MAX];  /* 0
} MPI2_CONFIG_PAGE_SASIOUNIT_0,
_____unchanged_portion_omitted_
  Mpi2SasIOUnit1PhyData_t, MPI2_POINTER pMpi2SasIOUnit1PhyData_t;

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumPhys at runtime.
 * one and check Header.ExtPageLength or NumPhys at runtime.
 */
#ifndef MPI2_SAS_IOUNIT1_PHY_MAX
```

```
#define MPI2_SAS_IOUNIT1_PHY_MAX        (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_1
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                         /* 0
    U16                                 ControlFlags;                   /* 0
    U16                                 SASNarrowMaxQueueDepth;         /* 0
    U16                                 AdditionalControlFlags;         /* 0
    U16                                 SASWideMaxQueueDepth;           /* 0
    U8                                  NumPhys;                        /* 0
    U8                                  SATAMaxQDepth;                  /* 0
    U8                                  ReportDeviceMissingDelay;       /* 0
    U8                                  IODeviceMissingDelay;           /* 0
    MPI2_SAS_IO_UNIT1_PHY_DATA          PhyData[MPI2_SAS_IOUNIT1_PHY_MAX];  /* 0
} MPI2_CONFIG_PAGE_SASIOUNIT_1,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_1,
  Mpi2SasIOUnitPage1_t, MPI2_POINTER pMpi2SasIOUnitPage1_t;

#define MPI2_SASIOUNITPAGE1_PAGEVERSION     (0x09)

/* values for SAS IO Unit Page 1 ControlFlags */
#define MPI2_SASIOUNIT1_CONTROL_DEVICE_SELF_TEST                    (0x8000)
#define MPI2_SASIOUNIT1_CONTROL_SATA_3_0_MAX                        (0x4000)
#define MPI2_SASIOUNIT1_CONTROL_SATA_1_5_MAX                        (0x2000) /*
#define MPI2_SASIOUNIT1_CONTROL_SATA_1_5_MAX                        (0x2000)
#define MPI2_SASIOUNIT1_CONTROL_SATA_SW_PRESERVE                    (0x1000)

#define MPI2_SASIOUNIT1_CONTROL_MASK_DEV_SUPPORT                    (0x0600)
#define MPI2_SASIOUNIT1_CONTROL_SHIFT_DEV_SUPPORT                   (9)
#define MPI2_SASIOUNIT1_CONTROL_DEV_SUPPORT_BOTH                    (0x0)
#define MPI2_SASIOUNIT1_CONTROL_DEV_SAS_SUPPORT                     (0x1)
#define MPI2_SASIOUNIT1_CONTROL_DEV_SATA_SUPPORT                    (0x2)

#define MPI2_SASIOUNIT1_CONTROL_SATA_48BIT_LBA_REQUIRED             (0x0080)
#define MPI2_SASIOUNIT1_CONTROL_SATA_SMART_REQUIRED                 (0x0040)
#define MPI2_SASIOUNIT1_CONTROL_SATA_NCQ_REQUIRED                   (0x0020)
#define MPI2_SASIOUNIT1_CONTROL_SATA_FUA_REQUIRED                   (0x0010)
#define MPI2_SASIOUNIT1_CONTROL_TABLE_SUBTRACTIVE_ILLEGAL           (0x0008)
#define MPI2_SASIOUNIT1_CONTROL_SUBTRACTIVE_ILLEGAL                 (0x0004)
#define MPI2_SASIOUNIT1_CONTROL_FIRST_LVL_DISC_ONLY                 (0x0002)
#define MPI2_SASIOUNIT1_CONTROL_CLEAR_AFFILIATION                   (0x0001) /*
#define MPI2_SASIOUNIT1_CONTROL_CLEAR_AFFILIATION                   (0x0001)

/* values for SAS IO Unit Page 1 AdditionalControlFlags */
#define MPI2_SASIOUNIT1_ACONTROL_MULTI_PORT_DOMAIN_ILLEGAL          (0x0080)
#define MPI2_SASIOUNIT1_ACONTROL_SATA_ASYNCHROUNOUS_NOTIFICATION    (0x0040)
#define MPI2_SASIOUNIT1_ACONTROL_INVALID_TOPOLOGY_CORRECTION        (0x0020)
#define MPI2_SASIOUNIT1_ACONTROL_PORT_ENABLE_ONLY_SATA_LINK_RESET   (0x0010)
#define MPI2_SASIOUNIT1_ACONTROL_OTHER_AFFILIATION_SATA_LINK_RESET  (0x0008)
#define MPI2_SASIOUNIT1_ACONTROL_SELF_AFFILIATION_SATA_LINK_RESET   (0x0004)
#define MPI2_SASIOUNIT1_ACONTROL_NO_AFFILIATION_SATA_LINK_RESET     (0x0002)
#define MPI2_SASIOUNIT1_ACONTROL_ALLOW_TABLE_TO_TABLE               (0x0001)

/* defines for SAS IO Unit Page 1 ReportDeviceMissingDelay */
#define MPI2_SASIOUNIT1_REPORT_MISSING_TIMEOUT_MASK                 (0x7F)
#define MPI2_SASIOUNIT1_REPORT_MISSING_UNIT_16                      (0x80)

/* values for SAS IO Unit Page 1 PortFlags */
#define MPI2_SASIOUNIT1_PORT_FLAGS_AUTO_PORT_CONFIG                 (0x01)

/* values for SAS IO Unit Page 1 PhyFlags */
#define MPI2_SASIOUNIT1_PHYFLAGS_ZONING_ENABLE                      (0x10)
#define MPI2_SASIOUNIT1_PHYFLAGS_PHY_DISABLE                        (0x08)

/* values for SAS IO Unit Page 1 MaxMinLinkRate */
```



```
#define MPI2_SASIOUNIT1_MAX_RATE_MASK                               (0xF0)
#define MPI2_SASIOUNIT1_MAX_RATE_1_5                                (0x80)
#define MPI2_SASIOUNIT1_MAX_RATE_3_0                                (0x90)
#define MPI2_SASIOUNIT1_MAX_RATE_6_0                                (0xA0)
#define MPI25_SASIOUNIT1_MAX_RATE_12_0                              (0xB0)
#define MPI2_SASIOUNIT1_MIN_RATE_MASK                               (0x0F)
#define MPI2_SASIOUNIT1_MIN_RATE_1_5                                (0x08)
#define MPI2_SASIOUNIT1_MIN_RATE_3_0                                (0x09)
#define MPI2_SASIOUNIT1_MIN_RATE_6_0                                (0x0A)
#define MPI25_SASIOUNIT1_MIN_RATE_12_0                              (0x0B)

/* see mpi2_sas.h for values for SAS IO Unit Page 1 ControllerPhyDeviceInfo valu


/* SAS IO Unit Page 4 */

typedef struct _MPI2_SAS_IOUNIT4_SPINUP_GROUP
{
    U8          MaxTargetSpinup;            /* 0x00 */
    U8          SpinupDelay;                /* 0x01 */
    U8          SpinupFlags;                /* 0x02 */
    U8          Reserved1;                  /* 0x03 */
    U16         Reserved1;                  /* 0x02 */
} MPI2_SAS_IOUNIT4_SPINUP_GROUP, MPI2_POINTER PTR_MPI2_SAS_IOUNIT4_SPINUP_GROUP,
  Mpi2SasIOUnit4SpinupGroup_t, MPI2_POINTER pMpi2SasIOUnit4SpinupGroup_t;

/* defines for SAS IO Unit Page 4 SpinupFlags */
#define MPI2_SASIOUNIT4_SPINUP_DISABLE_FLAG         (0x01)


/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumPhys at runtime.
 * four and check Header.ExtPageLength or NumPhys at runtime.
 */
#ifndef MPI2_SAS_IOUNIT4_PHY_MAX
#define MPI2_SAS_IOUNIT4_PHY_MAX        (4)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_4
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                         /* 0x00
    MPI2_SAS_IOUNIT4_SPINUP_GROUP       SpinupGroupParameters[4];       /* 0x08
    U32                                 Reserved1;                      /* 0x18
    U32                                 Reserved2;                      /* 0x1C
    U32                                 Reserved3;                      /* 0x20
    U8                                  BootDeviceWaitTime;             /* 0x24
    U8                                  Reserved4;                      /* 0x25
    U16                                 Reserved5;                      /* 0x26
    U8                                  NumPhys;                        /* 0x28
    U8                                  PEInitialSpinupDelay;           /* 0x29
    U8                                  PEReplyDelay;                   /* 0x2A
    U8                                  Flags;                          /* 0x2B
    U8                                  PHY[MPI2_SAS_IOUNIT4_PHY_MAX];  /* 0x2C
} MPI2_CONFIG_PAGE_SASIOUNIT_4,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_4,
  Mpi2SasIOUnitPage4_t, MPI2_POINTER pMpi2SasIOUnitPage4_t;

#define MPI2_SASIOUNITPAGE4_PAGEVERSION     (0x02)

/* defines for Flags field */
#define MPI2_SASIOUNIT4_FLAGS_AUTO_PORTENABLE               (0x01)

/* defines for PHY field */
#define MPI2_SASIOUNIT4_PHY_SPINUP_GROUP_MASK               (0x03)
```

```
/* SAS IO Unit Page 5 */

typedef struct _MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS
{
    U8          ControlFlags;               /* 0x00 */
    U8          PortWidthModGroup;          /* 0x01 */
    U8          Reserved1;                  /* 0x01 */
    U16         InactivityTimerExponent;    /* 0x02 */
    U8          SATAPartialTimeout;         /* 0x04 */
    U8          Reserved2;                  /* 0x05 */
    U8          SATASlumberTimeout;         /* 0x06 */
    U8          Reserved3;                  /* 0x07 */
    U8          SASPartialTimeout;          /* 0x08 */
    U8          Reserved4;                  /* 0x09 */
    U8          SASSlumberTimeout;          /* 0x0A */
    U8          Reserved5;                  /* 0x0B */
} MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS,
  MPI2_POINTER PTR_MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS,
  Mpi2SasIOUnit5PhyPmSettings_t, MPI2_POINTER pMpi2SasIOUnit5PhyPmSettings_t;

/* defines for ControlFlags field */
#define MPI2_SASIOUNIT5_CONTROL_SAS_SLUMBER_ENABLE      (0x08)
#define MPI2_SASIOUNIT5_CONTROL_SAS_PARTIAL_ENABLE      (0x04)
#define MPI2_SASIOUNIT5_CONTROL_SATA_SLUMBER_ENABLE     (0x02)
#define MPI2_SASIOUNIT5_CONTROL_SATA_PARTIAL_ENABLE     (0x01)

/* defines for PortWidthModeGroup field */
#define MPI2_SASIOUNIT5_PWMG_DISABLE                    (0xFF)

/* defines for InactivityTimerExponent field */
#define MPI2_SASIOUNIT5_ITE_MASK_SAS_SLUMBER            (0x7000)
#define MPI2_SASIOUNIT5_ITE_SHIFT_SAS_SLUMBER           (12)
#define MPI2_SASIOUNIT5_ITE_MASK_SAS_PARTIAL            (0x0700)
#define MPI2_SASIOUNIT5_ITE_SHIFT_SAS_PARTIAL           (8)
#define MPI2_SASIOUNIT5_ITE_MASK_SATA_SLUMBER           (0x0070)
#define MPI2_SASIOUNIT5_ITE_SHIFT_SATA_SLUMBER          (4)
#define MPI2_SASIOUNIT5_ITE_MASK_SATA_PARTIAL           (0x0007)
#define MPI2_SASIOUNIT5_ITE_SHIFT_SATA_PARTIAL          (0)

#define MPI2_SASIOUNIT5_ITE_TEN_SECONDS                 (7)
#define MPI2_SASIOUNIT5_ITE_ONE_SECOND                  (6)
#define MPI2_SASIOUNIT5_ITE_HUNDRED_MILLISECONDS        (5)
#define MPI2_SASIOUNIT5_ITE_TEN_MILLISECONDS            (4)
#define MPI2_SASIOUNIT5_ITE_ONE_MILLISECOND             (3)
#define MPI2_SASIOUNIT5_ITE_HUNDRED_MICROSECONDS        (2)
#define MPI2_SASIOUNIT5_ITE_TEN_MICROSECONDS            (1)
#define MPI2_SASIOUNIT5_ITE_ONE_MICROSECOND             (0)

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumPhys at runtime.
 * one and check Header.ExtPageLength or NumPhys at runtime.
 */
#ifndef MPI2_SAS_IOUNIT5_PHY_MAX
#define MPI2_SAS_IOUNIT5_PHY_MAX        (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_5
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                             /* 0
    U8                                  NumPhys;                            /* 0
    U8                                  Reserved1;                          /* 0
    U16                                 Reserved2;                          /* 0
    U32                                 Reserved3;                          /* 0
    MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS   SASPhyPowerManagementSettings[MPI2_SAS_I
```



```
} MPI2_CONFIG_PAGE_SASIOUNIT_5,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_5,
  Mpi2SasIOUnitPage5_t, MPI2_POINTER pMpi2SasIOUnitPage5_t;

#define MPI2_SASIOUNITPAGE5_PAGEVERSION     (0x01)
#define MPI2_SASIOUNITPAGE5_PAGEVERSION     (0x00)


/* SAS IO Unit Page 6 */

typedef struct _MPI2_SAS_IO_UNIT6_PORT_WIDTH_MOD_GROUP_STATUS
{
    U8          CurrentStatus;              /* 0x00 */
    U8          CurrentModulation;          /* 0x01 */
    U8          CurrentUtilization;         /* 0x02 */
    U8          Reserved1;                  /* 0x03 */
    U32         Reserved2;                  /* 0x04 */
} MPI2_SAS_IO_UNIT6_PORT_WIDTH_MOD_GROUP_STATUS,
  MPI2_POINTER PTR_MPI2_SAS_IO_UNIT6_PORT_WIDTH_MOD_GROUP_STATUS,
  Mpi2SasIOUnit6PortWidthModGroupStatus_t,
  MPI2_POINTER pMpi2SasIOUnit6PortWidthModGroupStatus_t;

/* defines for CurrentStatus field */
#define MPI2_SASIOUNIT6_STATUS_UNAVAILABLE                      (0x00)
#define MPI2_SASIOUNIT6_STATUS_UNCONFIGURED                     (0x01)
#define MPI2_SASIOUNIT6_STATUS_INVALID_CONFIG                   (0x02)
#define MPI2_SASIOUNIT6_STATUS_LINK_DOWN                        (0x03)
#define MPI2_SASIOUNIT6_STATUS_OBSERVATION_ONLY                 (0x04)
#define MPI2_SASIOUNIT6_STATUS_INACTIVE                         (0x05)
#define MPI2_SASIOUNIT6_STATUS_ACTIVE_IOUNIT                    (0x06)
#define MPI2_SASIOUNIT6_STATUS_ACTIVE_HOST                      (0x07)

/* defines for CurrentModulation field */
#define MPI2_SASIOUNIT6_MODULATION_25_PERCENT                   (0x00)
#define MPI2_SASIOUNIT6_MODULATION_50_PERCENT                   (0x01)
#define MPI2_SASIOUNIT6_MODULATION_75_PERCENT                   (0x02)
#define MPI2_SASIOUNIT6_MODULATION_100_PERCENT                  (0x03)

/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumGroups at runtime.
 */
#ifndef MPI2_SAS_IOUNIT6_GROUP_MAX
#define MPI2_SAS_IOUNIT6_GROUP_MAX      (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_6
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
    U32                                 Reserved1;                  /* 0x08 */
    U32                                 Reserved2;                  /* 0x0C */
    U8                                  NumGroups;                  /* 0x10 */
    U8                                  Reserved3;                  /* 0x11 */
    U16                                 Reserved4;                  /* 0x12 */
    MPI2_SAS_IO_UNIT6_PORT_WIDTH_MOD_GROUP_STATUS
        PortWidthModulationGroupStatus[MPI2_SAS_IOUNIT6_GROUP_MAX]; /* 0x14 */
} MPI2_CONFIG_PAGE_SASIOUNIT_6,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_6,
  Mpi2SasIOUnitPage6_t, MPI2_POINTER pMpi2SasIOUnitPage6_t;

#define MPI2_SASIOUNITPAGE6_PAGEVERSION     (0x00)


/* SAS IO Unit Page 7 */

typedef struct _MPI2_SAS_IO_UNIT7_PORT_WIDTH_MOD_GROUP_SETTINGS
```

```
{
    U8          Flags;                      /* 0x00 */
    U8          Reserved1;                  /* 0x01 */
    U16         Reserved2;                  /* 0x02 */
    U8          Threshold75Pct;             /* 0x04 */
    U8          Threshold50Pct;             /* 0x05 */
    U8          Threshold25Pct;             /* 0x06 */
    U8          Reserved3;                  /* 0x07 */
} MPI2_SAS_IO_UNIT7_PORT_WIDTH_MOD_GROUP_SETTINGS,
  MPI2_POINTER PTR_MPI2_SAS_IO_UNIT7_PORT_WIDTH_MOD_GROUP_SETTINGS,
  Mpi2SasIOUnit7PortWidthModGroupSettings_t,
  MPI2_POINTER pMpi2SasIOUnit7PortWidthModGroupSettings_t;

/* defines for Flags field */
#define MPI2_SASIOUNIT7_FLAGS_ENABLE_PORT_WIDTH_MODULATION  (0x01)


/*
 * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
 * one and check the value returned for NumGroups at runtime.
 */
#ifndef MPI2_SAS_IOUNIT7_GROUP_MAX
#define MPI2_SAS_IOUNIT7_GROUP_MAX      (1)
#endif

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_7
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER            Header;             /* 0x00 */
    U8                                          SamplingInterval;   /* 0x08 */
    U8                                          WindowLength;       /* 0x09 */
    U16                                         Reserved1;          /* 0x0A */
    U32                                         Reserved2;          /* 0x0C */
    U32                                         Reserved3;          /* 0x10 */
    U8                                          NumGroups;          /* 0x14 */
    U8                                          Reserved4;          /* 0x15 */
    U16                                         Reserved5;          /* 0x16 */
    MPI2_SAS_IO_UNIT7_PORT_WIDTH_MOD_GROUP_SETTINGS
        PortWidthModulationGroupSettings[MPI2_SAS_IOUNIT7_GROUP_MAX]; /* 0x18 */
} MPI2_CONFIG_PAGE_SASIOUNIT_7,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_7,
  Mpi2SasIOUnitPage7_t, MPI2_POINTER pMpi2SasIOUnitPage7_t;

#define MPI2_SASIOUNITPAGE7_PAGEVERSION     (0x00)


/* SAS IO Unit Page 8 */

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT_8
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                         /* 0x00
    U32                                 Reserved1;                      /* 0x08
    U32                                 PowerManagementCapabilities;    /* 0x0C
    U8                                  TxRxSleepStatus;                /* 0x10
    U8                                  Reserved2;                      /* 0x11
    U16                                 Reserved3;                      /* 0x12
} MPI2_CONFIG_PAGE_SASIOUNIT_8,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT_8,
  Mpi2SasIOUnitPage8_t, MPI2_POINTER pMpi2SasIOUnitPage8_t;

#define MPI2_SASIOUNITPAGE8_PAGEVERSION     (0x00)

/* defines for PowerManagementCapabilities field */
#define MPI2_SASIOUNIT8_PM_HOST_PORT_WIDTH_MOD          (0x00001000)
#define MPI2_SASIOUNIT8_PM_HOST_SAS_SLUMBER_MODE        (0x00000800)
#define MPI2_SASIOUNIT8_PM_HOST_SAS_PARTIAL_MODE        (0x00000400)
#define MPI2_SASIOUNIT8_PM_HOST_SATA_SLUMBER_MODE       (0x00000200)
```



```
#define MPI2_SASIOUNIT8_PM_HOST_SATA_PARTIAL_MODE       (0x00000100)
#define MPI2_SASIOUNIT8_PM_IOUNIT_PORT_WIDTH_MOD        (0x00000010)
#define MPI2_SASIOUNIT8_PM_IOUNIT_SAS_SLUMBER_MODE      (0x00000008)
#define MPI2_SASIOUNIT8_PM_IOUNIT_SAS_PARTIAL_MODE      (0x00000004)
#define MPI2_SASIOUNIT8_PM_IOUNIT_SATA_SLUMBER_MODE     (0x00000002)
#define MPI2_SASIOUNIT8_PM_IOUNIT_SATA_PARTIAL_MODE     (0x00000001)

/* defines for TxRxSleepStatus field */
#define MPI25_SASIOUNIT8_TXRXSLEEP_UNSUPPORTED          (0x00)
#define MPI25_SASIOUNIT8_TXRXSLEEP_DISENGAGED           (0x01)
#define MPI25_SASIOUNIT8_TXRXSLEEP_ACTIVE               (0x02)
#define MPI25_SASIOUNIT8_TXRXSLEEP_SHUTDOWN             (0x03)



/* SAS IO Unit Page 16 */

typedef struct _MPI2_CONFIG_PAGE_SASIOUNIT16
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                         /* 0
    U64                                 TimeStamp;                      /* 0
    U32                                 Reserved1;                      /* 0
    U32                                 Reserved2;                      /* 0
    U32                                 FastPathPendedRequests;         /* 0
    U32                                 FastPathUnPendedRequests;       /* 0
    U32                                 FastPathHostRequestStarts;      /* 0
    U32                                 FastPathFirmwareRequestStarts;  /* 0
    U32                                 FastPathHostCompletions;        /* 0
    U32                                 FastPathFirmwareCompletions;    /* 0
    U32                                 NonFastPathRequestStarts;       /* 0
    U32                                 NonFastPathHostCompletions;     /* 0
} MPI2_CONFIG_PAGE_SASIOUNIT16,
  MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SASIOUNIT16,
  Mpi2SasIOUnitPage16_t, MPI2_POINTER pMpi2SasIOUnitPage16_t;

#define MPI2_SASIOUNITPAGE16_PAGEVERSION    (0x00)


/*****************************************************************************
*   SAS Expander Config Pages
*****************************************************************************/

/* SAS Expander Page 0 */

typedef struct _MPI2_CONFIG_PAGE_EXPANDER_0
{
    MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
    U8                                  PhysicalPort;               /* 0x08 */
    U8                                  ReportGenLength;            /* 0x09 */
    U16                                 EnclosureHandle;            /* 0x0A */
    U64                                 SASAddress;                 /* 0x0C */
    U32                                 DiscoveryStatus;            /* 0x14 */
    U16                                 DevHandle;                  /* 0x18 */
    U16                                 ParentDevHandle;            /* 0x1A */
    U16                                 ExpanderChangeCount;        /* 0x1C */
    U16                                 ExpanderRouteIndexes;       /* 0x1E */
    U8                                  NumPhys;                    /* 0x20 */
    U8                                  SASLevel;                   /* 0x21 */
    U16                                 Flags;                      /* 0x22 */
    U16                                 STPBusInactivityTimeLimit;  /* 0x24 */
    U16                                 STPMaxConnectTimeLimit;     /* 0x26 */
    U16                                 STP_SMP_NexusLossTime;      /* 0x28 */
    U16                                 MaxNumRoutedSasAddresses;   /* 0x2A */
    U64                                 ActiveZoneManagerSASAddress;/* 0x2C */
    U16                                 ZoneLockInactivityLimit;    /* 0x34 */
    U16                                 Reserved1;                  /* 0x36 */
```

```
2425     U8                                  TimeToReducedFunc;          /* 0x38 */
2426     U8                                  InitialTimeToReducedFunc;   /* 0x39 */
2427     U8                                  MaxReducedFuncTime;         /* 0x3A */
2428     U8                                  Reserved2;                  /* 0x3B */
2429 } MPI2_CONFIG_PAGE_EXPANDER_0, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_EXPANDER_0,
_____unchanged_portion_omitted_
2498   Mpi2ExpanderPage1_t, MPI2_POINTER pMpi2ExpanderPage1_t;

2500 #define MPI2_SASEXPANDER1_PAGEVERSION       (0x02)

2502 /* use MPI2_SAS_PRATE_ defines for the ProgrammedLinkRate field */

2504 /* use MPI2_SAS_HWRATE_ defines for the HwLinkRate field */

2506 /* use MPI2_SAS_PHYINFO_ for the PhyInfo field */

2508 /* see mpi2_sas.h for the MPI2_SAS_DEVICE_INFO_ defines used for the AttachedDev

2510 /* use MPI2_SAS_NEG_LINK_RATE_ defines for the NegotiatedLinkRate field */

2060 /* use MPI2_SAS_APHYINFO_ defines for AttachedPhyInfo field */

2512 /* values for SAS Expander Page 1 DiscoveryInfo field */
2513 #define MPI2_SAS_EXPANDER1_DISCINFO_BAD_PHY_DISABLED    (0x04)
2514 #define MPI2_SAS_EXPANDER1_DISCINFO_LINK_STATUS_CHANGE  (0x02)
2515 #define MPI2_SAS_EXPANDER1_DISCINFO_NO_ROUTING_ENTRIES  (0x01)

2517 /* use MPI2_SAS_APHYINFO_ defines for AttachedPhyInfo field */


2520 /*****************************************************************************
2521 *   SAS Device Config Pages
2522 *****************************************************************************/

2524 /* SAS Device Page 0 */

2526 typedef struct _MPI2_CONFIG_PAGE_SAS_DEV_0
2527 {
2528     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                 /* 0x00 */
2529     U16                                 Slot;                   /* 0x08 */
2530     U16                                 EnclosureHandle;        /* 0x0A */
2531     U64                                 SASAddress;             /* 0x0C */
2532     U16                                 ParentDevHandle;        /* 0x14 */
2533     U8                                  PhyNum;                 /* 0x16 */
2534     U8                                  AccessStatus;           /* 0x17 */
2535     U16                                 DevHandle;              /* 0x18 */
2536     U8                                  AttachedPhyIdentifier;  /* 0x1A */
2537     U8                                  ZoneGroup;              /* 0x1B */
2538     U32                                 DeviceInfo;             /* 0x1C */
2539     U16                                 Flags;                  /* 0x20 */
2540     U8                                  PhysicalPort;           /* 0x22 */
2541     U8                                  MaxPortConnections;     /* 0x23 */
2542     U64                                 DeviceName;             /* 0x24 */
2543     U8                                  PortGroups;             /* 0x2C */
2544     U8                                  DmaGroup;               /* 0x2D */
2545     U8                                  ControlGroup;           /* 0x2E */
2546     U8                                  EnclosureLevel;         /* 0x2F */
2547     U8                                  ConnectorName[4];       /* 0x30 */
2094     U8                                  Reserved1;              /* 0x2F */
2095     U32                                 Reserved2;              /* 0x30 */
2548     U32                                 Reserved3;              /* 0x34 */
2549 } MPI2_CONFIG_PAGE_SAS_DEV_0, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_DEV_0,
2550   Mpi2SasDevicePage0_t, MPI2_POINTER pMpi2SasDevicePage0_t;

2552 #define MPI2_SASDEVICE0_PAGEVERSION         (0x09)
2100 #define MPI2_SASDEVICE0_PAGEVERSION         (0x08)
```



```
2554 /* values for SAS Device Page 0 AccessStatus field */
2555 #define MPI2_SAS_DEVICE0_ASTATUS_NO_ERRORS                  (0x00)
2556 #define MPI2_SAS_DEVICE0_ASTATUS_SATA_INIT_FAILED           (0x01)
2557 #define MPI2_SAS_DEVICE0_ASTATUS_SATA_CAPABILITY_FAILED     (0x02)
2558 #define MPI2_SAS_DEVICE0_ASTATUS_SATA_AFFILIATION_CONFLICT  (0x03)
2559 #define MPI2_SAS_DEVICE0_ASTATUS_SATA_NEEDS_INITIALIZATION  (0x04)
2560 #define MPI2_SAS_DEVICE0_ASTATUS_ROUTE_NOT_ADDRESSABLE      (0x05)
2561 #define MPI2_SAS_DEVICE0_ASTATUS_SMP_ERROR_NOT_ADDRESSABLE  (0x06)
2562 #define MPI2_SAS_DEVICE0_ASTATUS_DEVICE_BLOCKED             (0x07)
2563 /* specific values for SATA Init failures */
2564 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_UNKNOWN                (0x10)
2565 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_AFFILIATION_CONFLICT   (0x11)
2566 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_DIAG                   (0x12)
2567 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_IDENTIFICATION         (0x13)
2568 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_CHECK_POWER            (0x14)
2569 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_PIO_SN                 (0x15)
2570 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_MDMA_SN                (0x16)
2571 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_UDMA_SN                (0x17)
2572 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_ZONING_VIOLATION       (0x18)
2573 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_NOT_ADDRESSABLE        (0x19)
2574 #define MPI2_SAS_DEVICE0_ASTATUS_SIF_MAX                    (0x1F)

2576 /* see mpi2_sas.h for values for SAS Device Page 0 DeviceInfo values */

2578 /* values for SAS Device Page 0 Flags field */
2579 #define MPI2_SAS_DEVICE0_FLAGS_UNAUTHORIZED_DEVICE          (0x8000)
2580 #define MPI25_SAS_DEVICE0_FLAGS_ENABLED_FAST_PATH           (0x4000)
2581 #define MPI25_SAS_DEVICE0_FLAGS_FAST_PATH_CAPABLE           (0x2000)
2582 #define MPI2_SAS_DEVICE0_FLAGS_SLUMBER_PM_CAPABLE           (0x1000)
2583 #define MPI2_SAS_DEVICE0_FLAGS_PARTIAL_PM_CAPABLE           (0x0800)
2584 #define MPI2_SAS_DEVICE0_FLAGS_SATA_ASYNCHRONOUS_NOTIFY     (0x0400)
2585 #define MPI2_SAS_DEVICE0_FLAGS_SATA_SW_PRESERVE             (0x0200)
2586 #define MPI2_SAS_DEVICE0_FLAGS_UNSUPPORTED_DEVICE           (0x0100)
2587 #define MPI2_SAS_DEVICE0_FLAGS_SATA_48BIT_LBA_SUPPORTED     (0x0080)
2588 #define MPI2_SAS_DEVICE0_FLAGS_SATA_SMART_SUPPORTED         (0x0040)
2589 #define MPI2_SAS_DEVICE0_FLAGS_SATA_NCQ_SUPPORTED           (0x0020)
2590 #define MPI2_SAS_DEVICE0_FLAGS_SATA_FUA_SUPPORTED           (0x0010)
2591 #define MPI2_SAS_DEVICE0_FLAGS_PORT_SELECTOR_ATTACH         (0x0008)
2592 #define MPI2_SAS_DEVICE0_FLAGS_ENCL_LEVEL_VALID             (0x0002)
2593 #define MPI2_SAS_DEVICE0_FLAGS_DEVICE_PRESENT               (0x0001)


2596 /* SAS Device Page 1 */

2598 typedef struct _MPI2_CONFIG_PAGE_SAS_DEV_1
2599 {
2600     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                 /* 0x00 */
2601     U32                                 Reserved1;              /* 0x08 */
2602     U64                                 SASAddress;             /* 0x0C */
2603     U32                                 Reserved2;              /* 0x14 */
2604     U16                                 DevHandle;              /* 0x18 */
2605     U16                                 Reserved3;              /* 0x1A */
2606     U8                                  InitialRegDeviceFIS[20];/* 0x1C */
2607 } MPI2_CONFIG_PAGE_SAS_DEV_1, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_DEV_1,
_____unchanged_portion_omitted_
2637   Mpi2SasPhyPage0_t, MPI2_POINTER pMpi2SasPhyPage0_t;

2639 #define MPI2_SASPHY0_PAGEVERSION            (0x03)

2641 /* use MPI2_SAS_APHYINFO_ defines for AttachedPhyInfo field */

2643 /* use MPI2_SAS_PRATE_ defines for the ProgrammedLinkRate field */

2645 /* use MPI2_SAS_HWRATE_ defines for the HwLinkRate field */
```

```
2647 /* values for SAS PHY Page 0 Flags field */
2648 #define MPI2_SAS_PHY0_FLAGS_SGPIO_DIRECT_ATTACH_ENC             (0x01)

2650 /* use MPI2_SAS_PHYINFO_ for the PhyInfo field */
2192 /* use MPI2_SAS_APHYINFO_ defines for AttachedPhyInfo field */

2652 /* use MPI2_SAS_NEG_LINK_RATE_ defines for the NegotiatedLinkRate field */

2196 /* use MPI2_SAS_PHYINFO_ for the PhyInfo field */


2655 /* SAS PHY Page 1 */

2657 typedef struct _MPI2_CONFIG_PAGE_SAS_PHY_1
2658 {
2659     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2660     U32                                 Reserved1;                  /* 0x08 */
2661     U32                                 InvalidDwordCount;          /* 0x0C */
2662     U32                                 RunningDisparityErrorCount; /* 0x10 */
2663     U32                                 LossDwordSynchCount;        /* 0x14 */
2664     U32                                 PhyResetProblemCount;       /* 0x18 */
2665 } MPI2_CONFIG_PAGE_SAS_PHY_1, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_PHY_1,
______unchanged_portion_omitted_
2680   Mpi2SasPhy2PhyEvent_t, MPI2_POINTER pMpi2SasPhy2PhyEvent_t;

2682 /* use MPI2_SASPHY3_EVENT_CODE_ for the PhyEventCode field */


2685 /*
2686  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
2687  * one and check the value returned for NumPhyEvents at runtime.
2231  * one and check Header.ExtPageLength or NumPhyEvents at runtime.
2688  */
2689 #ifndef MPI2_SASPHY2_PHY_EVENT_MAX
2690 #define MPI2_SASPHY2_PHY_EVENT_MAX      (1)
2691 #endif

2693 typedef struct _MPI2_CONFIG_PAGE_SAS_PHY_2
2694 {
2695     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2696     U32                                 Reserved1;                  /* 0x08 */
2697     U8                                  NumPhyEvents;               /* 0x0C */
2698     U8                                  Reserved2;                  /* 0x0D */
2699     U16                                 Reserved3;                  /* 0x0E */
2700     MPI2_SASPHY2_PHY_EVENT              PhyEvent[MPI2_SASPHY2_PHY_EVENT_MAX]; /*
2701 } MPI2_CONFIG_PAGE_SAS_PHY_2, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_PHY_2,
______unchanged_portion_omitted_
2722   Mpi2SasPhy3PhyEventConfig_t, MPI2_POINTER pMpi2SasPhy3PhyEventConfig_t;

2724 /* values for PhyEventCode field */
2725 #define MPI2_SASPHY3_EVENT_CODE_NO_EVENT                    (0x00)
2726 #define MPI2_SASPHY3_EVENT_CODE_INVALID_DWORD               (0x01)
2727 #define MPI2_SASPHY3_EVENT_CODE_RUNNING_DISPARITY_ERROR     (0x02)
2728 #define MPI2_SASPHY3_EVENT_CODE_LOSS_DWORD_SYNC             (0x03)
2729 #define MPI2_SASPHY3_EVENT_CODE_PHY_RESET_PROBLEM           (0x04)
2730 #define MPI2_SASPHY3_EVENT_CODE_ELASTICITY_BUF_OVERFLOW     (0x05)
2731 #define MPI2_SASPHY3_EVENT_CODE_RX_ERROR                    (0x06)
2732 #define MPI2_SASPHY3_EVENT_CODE_RX_ADDR_FRAME_ERROR         (0x20)
2733 #define MPI2_SASPHY3_EVENT_CODE_TX_AC_OPEN_REJECT           (0x21)
2734 #define MPI2_SASPHY3_EVENT_CODE_RX_AC_OPEN_REJECT           (0x22)
2735 #define MPI2_SASPHY3_EVENT_CODE_TX_RC_OPEN_REJECT           (0x23)
2736 #define MPI2_SASPHY3_EVENT_CODE_RX_RC_OPEN_REJECT           (0x24)
2737 #define MPI2_SASPHY3_EVENT_CODE_RX_AIP_PARTIAL_WAITING_ON   (0x25)
2738 #define MPI2_SASPHY3_EVENT_CODE_RX_AIP_CONNECT_WAITING_ON   (0x26)
2739 #define MPI2_SASPHY3_EVENT_CODE_TX_BREAK                    (0x27)
2740 #define MPI2_SASPHY3_EVENT_CODE_RX_BREAK                    (0x28)
```



```
2741 #define MPI2_SASPHY3_EVENT_CODE_BREAK_TIMEOUT               (0x29)
2742 #define MPI2_SASPHY3_EVENT_CODE_CONNECTION                  (0x2A)
2743 #define MPI2_SASPHY3_EVENT_CODE_PEAKTX_PATHWAY_BLOCKED      (0x2B)
2744 #define MPI2_SASPHY3_EVENT_CODE_PEAKTX_ARB_WAIT_TIME        (0x2C)
2745 #define MPI2_SASPHY3_EVENT_CODE_PEAK_ARB_WAIT_TIME          (0x2D)
2746 #define MPI2_SASPHY3_EVENT_CODE_PEAK_CONNECT_TIME           (0x2E)
2747 #define MPI2_SASPHY3_EVENT_CODE_TX_SSP_FRAMES               (0x40)
2748 #define MPI2_SASPHY3_EVENT_CODE_RX_SSP_FRAMES               (0x41)
2749 #define MPI2_SASPHY3_EVENT_CODE_TX_SSP_ERROR_FRAMES         (0x42)
2750 #define MPI2_SASPHY3_EVENT_CODE_RX_SSP_ERROR_FRAMES         (0x43)
2751 #define MPI2_SASPHY3_EVENT_CODE_TX_CREDIT_BLOCKED           (0x44)
2752 #define MPI2_SASPHY3_EVENT_CODE_RX_CREDIT_BLOCKED           (0x45)
2753 #define MPI2_SASPHY3_EVENT_CODE_TX_SATA_FRAMES              (0x50)
2754 #define MPI2_SASPHY3_EVENT_CODE_RX_SATA_FRAMES              (0x51)
2755 #define MPI2_SASPHY3_EVENT_CODE_SATA_OVERFLOW               (0x52)
2756 #define MPI2_SASPHY3_EVENT_CODE_TX_SMP_FRAMES               (0x60)
2757 #define MPI2_SASPHY3_EVENT_CODE_RX_SMP_FRAMES               (0x61)
2758 #define MPI2_SASPHY3_EVENT_CODE_RX_SMP_ERROR_FRAMES         (0x63)
2759 #define MPI2_SASPHY3_EVENT_CODE_HOTPLUG_TIMEOUT             (0xD0)
2760 #define MPI2_SASPHY3_EVENT_CODE_MISALIGNED_MUX_PRIMITIVE    (0xD1)
2761 #define MPI2_SASPHY3_EVENT_CODE_RX_AIP                      (0xD2)

2763 /* values for the CounterType field */
2764 #define MPI2_SASPHY3_COUNTER_TYPE_WRAPPING                  (0x00)
2765 #define MPI2_SASPHY3_COUNTER_TYPE_SATURATING                (0x01)
2766 #define MPI2_SASPHY3_COUNTER_TYPE_PEAK_VALUE                (0x02)

2768 /* values for the TimeUnits field */
2769 #define MPI2_SASPHY3_TIME_UNITS_10_MICROSECONDS             (0x00)
2770 #define MPI2_SASPHY3_TIME_UNITS_100_MICROSECONDS            (0x01)
2771 #define MPI2_SASPHY3_TIME_UNITS_1_MILLISECOND               (0x02)
2772 #define MPI2_SASPHY3_TIME_UNITS_10_MILLISECONDS             (0x03)

2774 /* values for the ThresholdFlags field */
2775 #define MPI2_SASPHY3_TFLAGS_PHY_RESET                       (0x0002)
2776 #define MPI2_SASPHY3_TFLAGS_EVENT_NOTIFY                    (0x0001)

2778 /*
2779  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
2780  * one and check the value returned for NumPhyEvents at runtime.
2324  * one and check Header.ExtPageLength or NumPhyEvents at runtime.
2781  */
2782 #ifndef MPI2_SASPHY3_PHY_EVENT_MAX
2783 #define MPI2_SASPHY3_PHY_EVENT_MAX      (1)
2784 #endif

2786 typedef struct _MPI2_CONFIG_PAGE_SAS_PHY_3
2787 {
2788     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2789     U32                                 Reserved1;                  /* 0x08 */
2790     U8                                  NumPhyEvents;               /* 0x0C */
2791     U8                                  Reserved2;                  /* 0x0D */
2792     U16                                 Reserved3;                  /* 0x0E */
2793     MPI2_SASPHY3_PHY_EVENT_CONFIG       PhyEventConfig[MPI2_SASPHY3_PHY_EVENT_MA
2794 } MPI2_CONFIG_PAGE_SAS_PHY_3, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_PHY_3,
2795   Mpi2SasPhyPage3_t, MPI2_POINTER pMpi2SasPhyPage3_t;

2797 #define MPI2_SASPHY3_PAGEVERSION            (0x00)


2800 /* SAS PHY Page 4 */

2802 typedef struct _MPI2_CONFIG_PAGE_SAS_PHY_4
2803 {
2804     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2805     U16                                 Reserved1;                  /* 0x08 */
```

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2806     U8                                  Reserved2;                  /* 0x0A */
2807     U8                                  Flags;                      /* 0x0B */
2808     U8                                  InitialFrame[28];           /* 0x0C */
2809 } MPI2_CONFIG_PAGE_SAS_PHY_4, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_PHY_4,
2810   Mpi2SasPhyPage4_t, MPI2_POINTER pMpi2SasPhyPage4_t;

2812 #define MPI2_SASPHY4_PAGEVERSION            (0x00)

2814 /* values for the Flags field */
2815 #define MPI2_SASPHY4_FLAGS_FRAME_VALID        (0x02)
2816 #define MPI2_SASPHY4_FLAGS_SATA_FRAME         (0x01)




2821 /****************************************************************************
2822 *   SAS Port Config Pages
2823 ****************************************************************************/

2825 /* SAS Port Page 0 */

2827 typedef struct _MPI2_CONFIG_PAGE_SAS_PORT_0
2828 {
2829     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2830     U8                                  PortNumber;                 /* 0x08 */
2831     U8                                  PhysicalPort;               /* 0x09 */
2832     U8                                  PortWidth;                  /* 0x0A */
2833     U8                                  PhysicalPortWidth;          /* 0x0B */
2834     U8                                  ZoneGroup;                  /* 0x0C */
2835     U8                                  Reserved1;                  /* 0x0D */
2836     U16                                 Reserved2;                  /* 0x0E */
2837     U64                                 SASAddress;                 /* 0x10 */
2838     U32                                 DeviceInfo;                 /* 0x18 */
2839     U32                                 Reserved3;                  /* 0x1C */
2840     U32                                 Reserved4;                  /* 0x20 */
2841 } MPI2_CONFIG_PAGE_SAS_PORT_0, MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_PORT_0,
2842   Mpi2SasPortPage0_t, MPI2_POINTER pMpi2SasPortPage0_t;

2844 #define MPI2_SASPORT0_PAGEVERSION           (0x00)

2846 /* see mpi2_sas.h for values for SAS Port Page 0 DeviceInfo values */


2849 /****************************************************************************
2850 *   SAS Enclosure Config Pages
2851 ****************************************************************************/

2853 /* SAS Enclosure Page 0 */

2855 typedef struct _MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0
2856 {
2857     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                     /* 0x00 */
2858     U32                                 Reserved1;                  /* 0x08 */
2859     U64                                 EnclosureLogicalID;         /* 0x0C */
2860     U16                                 Flags;                      /* 0x14 */
2861     U16                                 EnclosureHandle;            /* 0x16 */
2862     U16                                 NumSlots;                   /* 0x18 */
2863     U16                                 StartSlot;                  /* 0x1A */
2864     U8                                  Reserved2;                  /* 0x1C */
2865     U8                                  EnclosureLevel;             /* 0x1D */
2387     U16                                 Reserved2;                  /* 0x1C */
2866     U16                                 SEPDevHandle;               /* 0x1E */
2867     U32                                 Reserved3;                  /* 0x20 */
2868     U32                                 Reserved4;                  /* 0x24 */
2869 } MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0,
2870   MPI2_POINTER PTR_MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0,
```



```
2871   Mpi2SasEnclosurePage0_t, MPI2_POINTER pMpi2SasEnclosurePage0_t;

2873 #define MPI2_SASENCLOSURE0_PAGEVERSION      (0x04)
2395 #define MPI2_SASENCLOSURE0_PAGEVERSION      (0x03)

2875 /* values for SAS Enclosure Page 0 Flags field */
2876 #define MPI2_SAS_ENCLS0_FLAGS_ENCL_LEVEL_VALID      (0x0010)
2877 #define MPI2_SAS_ENCLS0_FLAGS_MNG_MASK              (0x000F)
2878 #define MPI2_SAS_ENCLS0_FLAGS_MNG_UNKNOWN           (0x0000)
2879 #define MPI2_SAS_ENCLS0_FLAGS_MNG_IOC_SES           (0x0001)
2880 #define MPI2_SAS_ENCLS0_FLAGS_MNG_IOC_SGPIO         (0x0002)
2881 #define MPI2_SAS_ENCLS0_FLAGS_MNG_EXP_SGPIO         (0x0003)
2882 #define MPI2_SAS_ENCLS0_FLAGS_MNG_SES_ENCLOSURE     (0x0004)
2883 #define MPI2_SAS_ENCLS0_FLAGS_MNG_IOC_GPIO          (0x0005)


2886 /****************************************************************************
2887 *   Log Config Page
2888 ****************************************************************************/

2890 /* Log Page 0 */

2892 /*
2893  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
2894  * one and check the value returned for NumLogEntries at runtime.
2415  * one and check Header.ExtPageLength or NumPhys at runtime.
2895  */
2896 #ifndef MPI2_LOG_0_NUM_LOG_ENTRIES
2897 #define MPI2_LOG_0_NUM_LOG_ENTRIES          (1)
2898 #endif

2900 #define MPI2_LOG_0_LOG_DATA_LENGTH          (0x1C)

2902 typedef struct _MPI2_LOG_0_ENTRY
2903 {
2904     U64         TimeStamp;                          /* 0x00 */
2905     U32         Reserved1;                          /* 0x08 */
2906     U16         LogSequence;                        /* 0x0C */
2907     U16         LogEntryQualifier;                  /* 0x0E */
2908     U8          VP_ID;                              /* 0x10 */
2909     U8          VF_ID;                              /* 0x11 */
2910     U16         Reserved2;                          /* 0x12 */
2911     U8          LogData[MPI2_LOG_0_LOG_DATA_LENGTH];/* 0x14 */
2912 } MPI2_LOG_0_ENTRY, MPI2_POINTER PTR_MPI2_LOG_0_ENTRY,
_____unchanged_portion_omitted_
2931   Mpi2LogPage0_t, MPI2_POINTER pMpi2LogPage0_t;

2933 #define MPI2_LOG_0_PAGEVERSION              (0x02)


2936 /****************************************************************************
2937 *   RAID Config Page
2938 ****************************************************************************/

2940 /* RAID Page 0 */

2942 /*
2943  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
2944  * one and check the value returned for NumElements at runtime.
2465  * one and check Header.ExtPageLength or NumPhys at runtime.
2945  */
2946 #ifndef MPI2_RAIDCONFIG0_MAX_ELEMENTS
2947 #define MPI2_RAIDCONFIG0_MAX_ELEMENTS       (1)
2948 #endif

2950 typedef struct _MPI2_RAIDCONFIG0_CONFIG_ELEMENT
```

```
2951 {
2952     U16                     ElementFlags;               /* 0x00 */
2953     U16                     VolDevHandle;               /* 0x02 */
2954     U8                      HotSparePool;               /* 0x04 */
2955     U8                      PhysDiskNum;                /* 0x05 */
2956     U16                     PhysDiskDevHandle;          /* 0x06 */
2957 } MPI2_RAIDCONFIG0_CONFIG_ELEMENT,
_____unchanged_portion_omitted_
3117   Mpi2EthernetPage1_t, MPI2_POINTER pMpi2EthernetPage1_t;

3119 #define MPI2_ETHERNETPAGE1_PAGEVERSION   (0x00)

3121 /* values for Ethernet Page 1 Flags field */
3122 #define MPI2_ETHPG1_FLAG_SET_DEFAULT_IF             (0x00000100)
3123 #define MPI2_ETHPG1_FLAG_ENABLE_FW_DOWNLOAD         (0x00000080)
3124 #define MPI2_ETHPG1_FLAG_ENABLE_TELNET              (0x00000040)
3125 #define MPI2_ETHPG1_FLAG_ENABLE_SSH2                (0x00000020)
3126 #define MPI2_ETHPG1_FLAG_ENABLE_DHCP_CLIENT         (0x00000010)
3127 #define MPI2_ETHPG1_FLAG_ENABLE_IPV6                (0x00000008)
3128 #define MPI2_ETHPG1_FLAG_ENABLE_IPV4                (0x00000004)
3129 #define MPI2_ETHPG1_FLAG_USE_IPV6_ADDRESSES         (0x00000002)
3130 #define MPI2_ETHPG1_FLAG_ENABLE_ETH_IF              (0x00000001)

3132 /* values for Ethernet Page 1 MediaState field */
3133 #define MPI2_ETHPG1_MS_DUPLEX_MASK                  (0x80)
3134 #define MPI2_ETHPG1_MS_HALF_DUPLEX                  (0x00)
3135 #define MPI2_ETHPG1_MS_FULL_DUPLEX                  (0x80)

3137 #define MPI2_ETHPG1_MS_DATA_RATE_MASK               (0x07)
3138 #define MPI2_ETHPG1_MS_DATA_RATE_AUTO               (0x00)
3139 #define MPI2_ETHPG1_MS_DATA_RATE_10MBIT             (0x01)
3140 #define MPI2_ETHPG1_MS_DATA_RATE_100MBIT            (0x02)
3141 #define MPI2_ETHPG1_MS_DATA_RATE_1GBIT              (0x03)


3144 /*****************************************************************************
3145 *   Extended Manufacturing Config Pages
3146 *****************************************************************************/

3148 /*
3149  * Generic structure to use for product-specific extended manufacturing pages
3150  * (currently Extended Manufacturing Page 40 through Extended Manufacturing
3151  * Page 60).
3152  */

3154 typedef struct _MPI2_CONFIG_PAGE_EXT_MAN_PS
3155 {
3156     MPI2_CONFIG_EXTENDED_PAGE_HEADER    Header;                 /* 0x00 */
3157     U32                                 ProductSpecificInfo;    /* 0x08 */
3158 } MPI2_CONFIG_PAGE_EXT_MAN_PS,
3159   MPI2_POINTER PTR_MPI2_CONFIG_PAGE_EXT_MAN_PS,
3160   Mpi2ExtManufacturingPagePS_t, MPI2_POINTER pMpi2ExtManufacturingPagePS_t;

3162 /* PageVersion should be provided by product-specific code */

3164 #endif
```

```
**********************************************************
    6995 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_hbd.h
NEX-1888 upstream
**********************************************************
```

```
/*-
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 */

/*
 *  Copyright (c) 2009-2011 LSI Corporation.
 *
 *
 *           Name:  mpi2_hbd.h
 *          Title:  MPI Host Based Discovery messages and structures
 *  Creation Date:  October 21, 2009
 *
 *  mpi2_hbd.h Version:  02.00.02
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  10-28-09  02.00.00  Initial version.
 *  08-11-10  02.00.01  Removed PortGroups, DmaGroup, and ControlGroup from
 *                      HBD Action request, replaced by AdditionalInfo field.
 *  11-18-11  02.00.02  Incorporating additions for MPI v2.5.
 *  ------------------------------------------------------------------------
 */

#ifndef MPI2_HBD_H
#define MPI2_HBD_H

/*****************************************************************************
*  Host Based Discovery Action messages
```



```
******************************************************************************/

/* Host Based Discovery Action Request Message */
typedef struct _MPI2_HBD_ACTION_REQUEST
{
    U8                      Operation;          /* 0x00 */
    U8                      Reserved1;          /* 0x01 */
    U8                      ChainOffset;        /* 0x02 */
    U8                      Function;           /* 0x03 */
    U16                     DevHandle;          /* 0x04 */
    U8                      Reserved2;          /* 0x06 */
    U8                      MsgFlags;           /* 0x07 */
    U8                      VP_ID;              /* 0x08 */
    U8                      VF_ID;              /* 0x09 */
    U16                     Reserved3;          /* 0x0A */
    U32                     Reserved4;          /* 0x0C */
    U64                     SASAddress;         /* 0x10 */
    U32                     Reserved5;          /* 0x18 */
    U32                     HbdDeviceInfo;      /* 0x1C */
    U16                     ParentDevHandle;    /* 0x20 */
    U16                     MaxQDepth;          /* 0x22 */
    U8                      FirstPhyIdentifier; /* 0x24 */
    U8                      Port;               /* 0x25 */
    U8                      MaxConnections;     /* 0x26 */
    U8                      MaxRate;            /* 0x27 */
    U32                     AdditionalInfo;     /* 0x28 */
    U16                     InitialAWT;         /* 0x2C */
    U16                     Reserved7;          /* 0x2E */
    U32                     Reserved8;          /* 0x30 */
} MPI2_HBD_ACTION_REQUEST, MPI2_POINTER PTR_MPI2_HBD_ACTION_REQUEST,
  Mpi2HbdActionRequest_t, MPI2_POINTER pMpi2HbdActionRequest_t;

/* values for the Operation field */
#define MPI2_HBD_OP_ADD_DEVICE                  (0x01)
#define MPI2_HBD_OP_REMOVE_DEVICE               (0x02)
#define MPI2_HBD_OP_UPDATE_DEVICE               (0x03)

/* values for the HbdDeviceInfo field */
#define MPI2_HBD_DEVICE_INFO_VIRTUAL_DEVICE     (0x00004000)
#define MPI2_HBD_DEVICE_INFO_ATAPI_DEVICE       (0x00002000)
#define MPI2_HBD_DEVICE_INFO_DIRECT_ATTACH      (0x00000800)
#define MPI2_HBD_DEVICE_INFO_SSP_TARGET         (0x00000400)
#define MPI2_HBD_DEVICE_INFO_STP_TARGET         (0x00000200)
#define MPI2_HBD_DEVICE_INFO_SMP_TARGET         (0x00000100)
#define MPI2_HBD_DEVICE_INFO_SATA_DEVICE        (0x00000080)
#define MPI2_HBD_DEVICE_INFO_SSP_INITIATOR      (0x00000040)
#define MPI2_HBD_DEVICE_INFO_STP_INITIATOR      (0x00000020)
#define MPI2_HBD_DEVICE_INFO_SMP_INITIATOR      (0x00000010)
#define MPI2_HBD_DEVICE_INFO_SATA_HOST          (0x00000008)

#define MPI2_HBD_DEVICE_INFO_MASK_DEVICE_TYPE   (0x00000007)
#define MPI2_HBD_DEVICE_INFO_NO_DEVICE          (0x00000000)
#define MPI2_HBD_DEVICE_INFO_END_DEVICE         (0x00000001)
#define MPI2_HBD_DEVICE_INFO_EDGE_EXPANDER      (0x00000002)
#define MPI2_HBD_DEVICE_INFO_FANOUT_EXPANDER    (0x00000003)

/* values for the MaxRate field */
#define MPI2_HBD_MAX_RATE_MASK                  (0x0F)
#define MPI2_HBD_MAX_RATE_1_5                   (0x08)
#define MPI2_HBD_MAX_RATE_3_0                   (0x09)
#define MPI2_HBD_MAX_RATE_6_0                   (0x0A)
#define MPI25_HBD_MAX_RATE_12_0                 (0x0B)


/* Host Based Discovery Action Reply Message */
typedef struct _MPI2_HBD_ACTION_REPLY
```

```
128 {
129     U8                      Operation;          /* 0x00 */
130     U8                      Reserved1;          /* 0x01 */
131     U8                      MsgLength;          /* 0x02 */
132     U8                      Function;           /* 0x03 */
133     U16                     DevHandle;          /* 0x04 */
134     U8                      Reserved2;          /* 0x06 */
135     U8                      MsgFlags;           /* 0x07 */
136     U8                      VP_ID;              /* 0x08 */
137     U8                      VF_ID;              /* 0x09 */
138     U16                     Reserved3;          /* 0x0A */
139     U16                     Reserved4;          /* 0x0C */
140     U16                     IOCStatus;          /* 0x0E */
141     U32                     IOCLogInfo;         /* 0x10 */
142 } MPI2_HBD_ACTION_REPLY, MPI2_POINTER PTR_MPI2_HBD_ACTION_REPLY,
143   Mpi2HbdActionReply_t, MPI2_POINTER pMpi2HbdActionReply_t;


146 #endif
```

```
**********************************************************
   37705 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_history.txt
NEX-1888 upstream
**********************************************************
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 */

 ==============================
 Fusion-MPT MPI 2.0 / 2.5 Header File Change History
 ==============================

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 ---------------------------------------
 Header Set Release Version:    02.00.33
 Header Set Release Date:       12-05-13
 ---------------------------------------

 Filename               Current version     Prior version
 ----------             ---------------     -------------
 mpi2.h                 02.00.33            02.00.32
 mpi2_cnfg.h            02.00.27            02.00.26
 mpi2_init.h            02.00.15            02.00.15
 mpi2_ioc.h             02.00.24            02.00.23
 mpi2_raid.h            02.00.10            02.00.10
 mpi2_sas.h             02.00.08            02.00.08
 mpi2_targ.h            02.00.06            02.00.06
 mpi2_tool.h            02.00.11            02.00.11
 mpi2_type.h            02.00.00            02.00.00
 mpi2_ra.h              02.00.00            02.00.00
 mpi2_hbd.h             02.00.02            02.00.02
 mpi2_history.txt       02.00.33            02.00.32


 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------

mpi2.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
```



```
 *  06-04-07  02.00.01  Bumped MPI2_HEADER_VERSION_UNIT.
 *  06-26-07  02.00.02  Bumped MPI2_HEADER_VERSION_UNIT.
 *  08-31-07  02.00.03  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Moved ReplyPostHostIndex register to offset 0x6C of the
 *                      MPI2_SYSTEM_INTERFACE_REGS and modified the define for
 *                      MPI2_REPLY_POST_HOST_INDEX_OFFSET.
 *                      Added union of request descriptors.
 *                      Added union of reply descriptors.
 *  10-31-07  02.00.04  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added define for MPI2_VERSION_02_00.
 *                      Fixed the size of the FunctionDependent5 field in the
 *                      MPI2_DEFAULT_REPLY structure.
 *  12-18-07  02.00.05  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Removed the MPI-defined Fault Codes and extended the
 *                      product specific codes up to 0xEFFF.
 *                      Added a sixth key value for the WriteSequence register
 *                      and changed the flush value to 0x0.
 *                      Added message function codes for Diagnostic Buffer Post
 *                      and Diagnsotic Release.
 *                      New IOCStatus define: MPI2_IOCSTATUS_DIAGNOSTIC_RELEASED
 *                      Moved MPI2_VERSION_UNION from mpi2_ioc.h.
 *  02-29-08  02.00.06  Bumped MPI2_HEADER_VERSION_UNIT.
 *  03-03-08  02.00.07  Bumped MPI2_HEADER_VERSION_UNIT.
 *  05-21-08  02.00.08  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added #defines for marking a reply descriptor as unused.
 *  06-27-08  02.00.09  Bumped MPI2_HEADER_VERSION_UNIT.
 *  10-02-08  02.00.10  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Moved LUN field defines from mpi2_init.h.
 *  01-19-09  02.00.11  Bumped MPI2_HEADER_VERSION_UNIT.
 *  05-06-09  02.00.12  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      In all request and reply descriptors, replaced VF_ID
 *                      field with MSIxIndex field.
 *                      Removed DevHandle field from
 *                      MPI2_SCSI_IO_SUCCESS_REPLY_DESCRIPTOR and made those
 *                      bytes reserved.
 *                      Added RAID Accelerator functionality.
 *  07-30-09  02.00.13  Bumped MPI2_HEADER_VERSION_UNIT.
 *  10-28-09  02.00.14  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added MSI-x index mask and shift for Reply Post Host
 *                      Index register.
 *                      Added function code for Host Based Discovery Action.
 *  02-10-10  02.00.15  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added define for MPI2_FUNCTION_PWR_MGMT_CONTROL.
 *                      Added defines for product-specific range of message
 *                      function codes, 0xF0 to 0xFF.
 *  05-12-10  02.00.16  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added alternative defines for the SGE Direction bit.
 *  08-11-10  02.00.17  Bumped MPI2_HEADER_VERSION_UNIT.
 *  11-10-10  02.00.18  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added MPI2_IEEE_SGE_FLAGS_SYSTEMPLBCPI_ADDR define.
 *  02-23-11  02.00.19  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added MPI2_FUNCTION_SEND_HOST_MESSAGE.
 *  03-09-11  02.00.20  Bumped MPI2_HEADER_VERSION_UNIT.
 *  05-25-11  02.00.21  Bumped MPI2_HEADER_VERSION_UNIT.
 *  08-24-11  02.00.22  Bumped MPI2_HEADER_VERSION_UNIT.
 *  11-18-11  02.00.23  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Incorporating additions for MPI v2.5.
 *  02-06-12  02.00.24  Bumped MPI2_HEADER_VERSION_UNIT.
 *  03-29-12  02.00.25  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added Hard Reset delay timings.
 *  07-10-12  02.00.26  Bumped MPI2_HEADER_VERSION_UNIT.
 *  07-26-12  02.00.27  Bumped MPI2_HEADER_VERSION_UNIT.
 *  11-27-12  02.00.28  Bumped MPI2_HEADER_VERSION_UNIT.
 *  12-20-12  02.00.29  Bumped MPI2_HEADER_VERSION_UNIT.
 *                      Added MPI25_SUP_REPLY_POST_HOST_INDEX_OFFSET.
 *  04-09-13  02.00.30  Bumped MPI2_HEADER_VERSION_UNIT.
```

```
 *  04-17-13  02.00.31  Bumped MPI2_HEADER_VERSION_UNIT.
 *  08-19-13  02.00.32  Bumped MPI2_HEADER_VERSION_UNIT.
 *  12-05-13  02.00.33  Bumped MPI2_HEADER_VERSION_UNIT.
 *  --------------------------------------------------------------------

mpi2_cnfg.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-04-07  02.00.01  Added defines for SAS IO Unit Page 2 PhyFlags.
 *                      Added Manufacturing Page 11.
 *                      Added MPI2_SAS_EXPANDER0_FLAGS_CONNECTOR_END_DEVICE
 *                      define.
 *  06-26-07  02.00.02  Adding generic structure for product-specific
 *                      Manufacturing pages: MPI2_CONFIG_PAGE_MANUFACTURING_PS.
 *                      Rework of BIOS Page 2 configuration page.
 *                      Fixed MPI2_BIOSPAGE2_BOOT_DEVICE to be a union of the
 *                      forms.
 *                      Added configuration pages IOC Page 8 and Driver
 *                      Persistent Mapping Page 0.
 *  08-31-07  02.00.03  Modified configuration pages dealing with Integrated
 *                      RAID (Manufacturing Page 4, RAID Volume Pages 0 and 1,
 *                      RAID Physical Disk Pages 0 and 1, RAID Configuration
 *                      Page 0).
 *                      Added new value for AccessStatus field of SAS Device
 *                      Page 0 (_SATA_NEEDS_INITIALIZATION).
 *  10-31-07  02.00.04  Added missing SEPDevHandle field to
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *  12-18-07  02.00.05  Modified IO Unit Page 0 to use 32-bit version fields for
 *                      NVDATA.
 *                      Modified IOC Page 7 to use masks and added field for
 *                      SASBroadcastPrimitiveMasks.
 *                      Added MPI2_CONFIG_PAGE_BIOS_4.
 *                      Added MPI2_CONFIG_PAGE_LOG_0.
 *  02-29-08  02.00.06  Modified various names to make them 32-character unique.
 *                      Added SAS Device IDs.
 *                      Updated Integrated RAID configuration pages including
 *                      Manufacturing Page 4, IOC Page 6, and RAID Configuration
 *                      Page 0.
 *  05-21-08  02.00.07  Added define MPI2_MANPAGE4_MIX_SSD_SAS_SATA.
 *                      Added define MPI2_MANPAGE4_PHYSDISK_128MB_COERCION.
 *                      Fixed define MPI2_IOCPAGE8_FLAGS_ENCLOSURE_SLOT_MAPPING.
 *                      Added missing MaxNumRoutedSasAddresses field to
 *                      MPI2_CONFIG_PAGE_EXPANDER_0.
 *                      Added SAS Port Page 0.
 *                      Modified structure layout for
 *                      MPI2_CONFIG_PAGE_DRIVER_MAPPING_0.
 *  06-27-08  02.00.08  Changed MPI2_CONFIG_PAGE_RD_PDISK_1 to use
 *                      MPI2_RAID_PHYS_DISK1_PATH_MAX to size the array.
 *  10-02-08  02.00.09  Changed MPI2_RAID_PGAD_CONFIGNUM_MASK from 0x0000FFFF
 *                      to 0x000000FF.
 *                      Added two new values for the Physical Disk Coercion Size
 *                      bits in the Flags field of Manufacturing Page 4.
 *                      Added product-specific Manufacturing pages 16 to 31.
 *                      Modified Flags bits for controlling write cache on SATA
 *                      drives in IO Unit Page 1.
 *                      Added new bit to AdditionalControlFlags of SAS IO Unit
 *                      Page 1 to control Invalid Topology Correction.
 *                      Added SupportedPhysDisks field to RAID Volume Page 1 and
 *                      added related defines.
 *                      Added additional defines for RAID Volume Page 0
 *                      VolumeStatusFlags field.
 *                      Modified meaning of RAID Volume Page 0 VolumeSettings
 *                      define for auto-configure of hot-swap drives.
 *                      Added PhysDiskAttributes field (and related defines) to
 *                      RAID Physical Disk Page 0.
 *                      Added MPI2_SAS_PHYINFO_PHY_VACANT define.
 *                      Added three new DiscoveryStatus bits for SAS IO Unit
```



```
 *                      Page 0 and SAS Expander Page 0.
 *                      Removed multiplexing information from SAS IO Unit pages.
 *                      Added BootDeviceWaitTime field to SAS IO Unit Page 4.
 *                      Removed Zone Address Resolved bit from PhyInfo and from
 *                      Expander Page 0 Flags field.
 *                      Added two new AccessStatus values to SAS Device Page 0
 *                      for indicating routing problems. Added 3 reserved words
 *                      to this page.
 *  01-19-09  02.00.10  Fixed defines for GPIOVal field of IO Unit Page 3.
 *                      Inserted missing reserved field into structure for IOC
 *                      Page 6.
 *                      Added more pending task bits to RAID Volume Page 0
 *                      VolumeStatusFlags defines.
 *                      Added MPI2_PHYSDISK0_STATUS_FLAG_NOT_CERTIFIED define.
 *                      Added a new DiscoveryStatus bit for SAS IO Unit Page 0
 *                      and SAS Expander Page 0 to flag a downstream initiator
 *                      when in simplified routing mode.
 *                      Removed SATA Init Failure defines for DiscoveryStatus
 *                      fields of SAS IO Unit Page 0 and SAS Expander Page 0.
 *                      Added MPI2_SAS_DEVICE0_ASTATUS_DEVICE_BLOCKED define.
 *                      Added PortGroups, DmaGroup, and ControlGroup fields to
 *                      SAS Device Page 0.
 *  05-06-09  02.00.11  Added structures and defines for IO Unit Page 5 and IO
 *                      Unit Page 6.
 *                      Added expander reduced functionality data to SAS
 *                      Expander Page 0.
 *                      Added SAS PHY Page 2 and SAS PHY Page 3.
 *  07-30-09  02.00.12  Added IO Unit Page 7.
 *                      Added new device ids.
 *                      Added SAS IO Unit Page 5.
 *                      Added partial and slumber power management capable flags
 *                      to SAS Device Page 0 Flags field.
 *                      Added PhyInfo defines for power condition.
 *                      Added Ethernet configuration pages.
 *  10-28-09  02.00.13  Added MPI2_IOUNITPAGE1_ENABLE_HOST_BASED_DISCOVERY.
 *                      Added SAS PHY Page 4 structure and defines.
 *  02-10-10  02.00.14  Modified the comments for the configuration page
 *                      structures that contain an array of data. The host
 *                      should use the "count" field in the page data (e.g. the
 *                      NumPhys field) to determine the number of valid elements
 *                      in the array.
 *                      Added/modified some MPI2_MFGPAGE_DEVID_SAS defines.
 *                      Added PowerManagementCapabilities to IO Unit Page 7.
 *                      Added PortWidthModGroup field to
 *                      MPI2_SAS_IO_UNIT5_PHY_PM_SETTINGS.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_6 and related defines.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_7 and related defines.
 *                      Added MPI2_CONFIG_PAGE_SASIOUNIT_8 and related defines.
 *  05-12-10  02.00.15  Added MPI2_RAIDVOL0_STATUS_FLAG_VOL_NOT_CONSISTENT
 *                      define.
 *                      Added MPI2_PHYSDISK0_INCOMPATIBLE_MEDIA_TYPE define.
 *                      Added MPI2_SAS_NEG_LINK_RATE_UNSUPPORTED_PHY define.
 *  08-11-10  02.00.16  Removed IO Unit Page 1 device path (multi-pathing)
 *                      defines.
 *  11-10-10  02.00.17  Added ReceptacleID field (replacing Reserved1) to
 *                      MPI2_MANPAGE7_CONNECTOR_INFO and reworked defines for
 *                      the Pinout field.
 *                      Added BoardTemperature and BoardTemperatureUnits fields
 *                      to MPI2_CONFIG_PAGE_IO_UNIT_7.
 *                      Added MPI2_CONFIG_EXTPAGETYPE_EXT_MANUFACTURING define
 *                      and MPI2_CONFIG_PAGE_EXT_MAN_PS structure.
 *  02-23-11  02.00.18  Added ProxyVF_ID field to MPI2_CONFIG_REQUEST.
 *                      Added IO Unit Page 8, IO Unit Page 9,
 *                      and IO Unit Page 10.
 *                      Added SASNotifyPrimitiveMasks field to
 *                      MPI2_CONFIG_PAGE_IOC_7.
```

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 *  03-09-11  02.00.19  Fixed IO Unit Page 10 (to match the spec).
 *  05-25-11  02.00.20  Cleaned up a few comments.
 *  08-24-11  02.00.21  Marked the IO Unit Page 7 PowerManagementCapabilities
 *                      for PCIe link as obsolete.
 *                      Added SpinupFlags field containing a Disable Spin-up bit
 *                      to the MPI2_SAS_IOUNIT4_SPINUP_GROUP fields of SAS IO
 *                      Unit Page 4.
 *  11-18-11  02.00.22  Added define MPI2_IOCPAGE6_CAP_FLAGS_4K_SECTORS_SUPPORT.
 *                      Added UEFIVersion field to BIOS Page 1 and defined new
 *                      BiosOptions bits.
 *                      Incorporating additions for MPI v2.5.
 *  11-27-12  02.00.23  Added MPI2_MANPAGE7_FLAG_EVENTREPLAY_SLOT_ORDER.
 *                      Added MPI2_BIOSPAGE1_OPTIONS_MASK_OEM_ID.
 *  12-20-12  02.00.24  Marked MPI2_SASIOUNIT1_CONTROL_CLEAR_AFFILIATION as
 *                      obsolete for MPI v2.5 and later.
 *                      Added some defines for 12G SAS speeds.
 *  04-09-13  02.00.25  Added MPI2_IOUNITPAGE1_ATA_SECURITY_FREEZE_LOCK.
 *                      Fixed MPI2_IOUNITPAGE5_DMA_CAP_MASK_MAX_REQUESTS to
 *                      match the specification.
 *  08-19-13  02.00.26  Added reserved words to MPI2_CONFIG_PAGE_IO_UNIT_7 for
 *                      future use.
 *  12-05-13  02.00.27  Added MPI2_MANPAGE7_FLAG_BASE_ENCLOSURE_LEVEL for
 *                      MPI2_CONFIG_PAGE_MAN_7.
 *                      Added EnclosureLevel and ConnectorName fields to
 *                      MPI2_CONFIG_PAGE_SAS_DEV_0.
 *                      Added MPI2_SAS_DEVICE0_FLAGS_ENCL_LEVEL_VALID for
 *                      MPI2_CONFIG_PAGE_SAS_DEV_0.
 *                      Added EnclosureLevel field to
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *                      Added MPI2_SAS_ENCLS0_FLAGS_ENCL_LEVEL_VALID for
 *                      MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0.
 *  ------------------------------------------------------------------------

mpi2_init.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  10-31-07  02.00.01  Fixed name for pMpi2SCSITaskManagementRequest_t.
 *  12-18-07  02.00.02  Modified Task Management Target Reset Method defines.
 *  02-29-08  02.00.03  Added Query Task Set and Query Unit Attention.
 *  03-03-08  02.00.04  Fixed name of struct _MPI2_SCSI_TASK_MANAGE_REPLY.
 *  05-21-08  02.00.05  Fixed typo in name of Mpi2SepRequest_t.
 *  10-02-08  02.00.06  Removed Untagged and No Disconnect values from SCSI IO
 *                      Control field Task Attribute flags.
 *                      Moved LUN field defines to mpi2.h becasue they are
 *                      common to many structures.
 *  05-06-09  02.00.07  Changed task management type of Query Unit Attention to
 *                      Query Asynchronous Event.
 *                      Defined two new bits in the SlotStatus field of the SCSI
 *                      Enclosure Processor Request and Reply.
 *  10-28-09  02.00.08  Added defines for decoding the ResponseInfo bytes for
 *                      both SCSI IO Error Reply and SCSI Task Management Reply.
 *                      Added ResponseInfo field to MPI2_SCSI_TASK_MANAGE_REPLY.
 *                      Added MPI2_SCSITASKMGMT_RSP_TM_OVERLAPPED_TAG define.
 *  02-10-10  02.00.09  Removed unused structure that had "#if 0" around it.
 *  05-12-10  02.00.10  Added optional vendor-unique region to SCSI IO Request.
 *  11-10-10  02.00.11  Added MPI2_SCSIIO_NUM_SGLOFFSETS define.
 *  11-18-11  02.00.12  Incorporating additions for MPI v2.5.
 *  02-06-12  02.00.13  Added alternate defines for Task Priority / Command
 *                      Priority to match SAM-4.
 *                      Added EEDPErrorOffset to MPI2_SCSI_IO_REPLY.
 *  07-10-12  02.00.14  Added MPI2_SCSIIO_CONTROL_SHIFT_DATADIRECTION.
 *  ------------------------------------------------------------------------

mpi2_ioc.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-04-07  02.00.01  In IOCFacts Reply structure, renamed MaxDevices to
 *                      MaxTargets.
```



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 *                      Added TotalImageSize field to FWDownload Request.
 *                      Added reserved words to FWUpload Request.
 *  06-26-07  02.00.02  Added IR Configuration Change List Event.
 *  08-31-07  02.00.03  Removed SystemReplyQueueDepth field from the IOCInit
 *                      request and replaced it with
 *                      ReplyDescriptorPostQueueDepth and ReplyFreeQueueDepth.
 *                      Replaced the MinReplyQueueDepth field of the IOCFacts
 *                      reply with MaxReplyDescriptorPostQueueDepth.
 *                      Added MPI2_RDPQ_DEPTH_MIN define to specify the minimum
 *                      depth for the Reply Descriptor Post Queue.
 *                      Added SASAddress field to Initiator Device Table
 *                      Overflow Event data.
 *  10-31-07  02.00.04  Added ReasonCode MPI2_EVENT_SAS_INIT_RC_NOT_RESPONDING
 *                      for SAS Initiator Device Status Change Event data.
 *                      Modified Reason Code defines for SAS Topology Change
 *                      List Event data, including adding a bit for PHY Vacant
 *                      status, and adding a mask for the Reason Code.
 *                      Added define for
 *                      MPI2_EVENT_SAS_TOPO_ES_DELAY_NOT_RESPONDING.
 *                      Added define for MPI2_EXT_IMAGE_TYPE_MEGARAID.
 *  12-18-07  02.00.05  Added Boot Status defines for the IOCExceptions field of
 *                      the IOCFacts Reply.
 *                      Removed MPI2_IOCFACTS_CAPABILITY_EXTENDED_BUFFER define.
 *                      Moved MPI2_VERSION_UNION to mpi2.h.
 *                      Changed MPI2_EVENT_NOTIFICATION_REQUEST to use masks
 *                      instead of enables, and added SASBroadcastPrimitiveMasks
 *                      field.
 *                      Added Log Entry Added Event and related structure.
 *  02-29-08  02.00.06  Added define MPI2_IOCFACTS_CAPABILITY_INTEGRATED_RAID.
 *                      Removed define MPI2_IOCFACTS_PROTOCOL_SMP_TARGET.
 *                      Added MaxVolumes and MaxPersistentEntries fields to
 *                      IOCFacts reply.
 *                      Added ProtocalFlags and IOCCapabilities fields to
 *                      MPI2_FW_IMAGE_HEADER.
 *                      Removed MPI2_PORTENABLE_FLAGS_ENABLE_SINGLE_PORT.
 *  03-03-08  02.00.07  Fixed MPI2_FW_IMAGE_HEADER by changing Reserved26 to
 *                      a U16 (from a U32).
 *                      Removed extra 's' from EventMasks name.
 *  06-27-08  02.00.08  Fixed an offset in a comment.
 *  10-02-08  02.00.09  Removed SystemReplyFrameSize from MPI2_IOC_INIT_REQUEST.
 *                      Removed CurReplyFrameSize from MPI2_IOC_FACTS_REPLY and
 *                      renamed MinReplyFrameSize to ReplyFrameSize.
 *                      Added MPI2_IOCFACTS_EXCEPT_IR_FOREIGN_CONFIG_MAX.
 *                      Added two new RAIDOperation values for Integrated RAID
 *                      Operations Status Event data.
 *                      Added four new IR Configuration Change List Event data
 *                      ReasonCode values.
 *                      Added two new ReasonCode defines for SAS Device Status
 *                      Change Event data.
 *                      Added three new DiscoveryStatus bits for the SAS
 *                      Discovery event data.
 *                      Added Multiplexing Status Change bit to the PhyStatus
 *                      field of the SAS Topology Change List event data.
 *                      Removed define for MPI2_INIT_IMAGE_BOOTFLAGS_XMEMCOPY.
 *                      BootFlags are now product-specific.
 *                      Added defines for the indivdual signature bytes
 *                      for MPI2_INIT_IMAGE_FOOTER.
 *  01-19-09  02.00.10  Added MPI2_IOCFACTS_CAPABILITY_EVENT_REPLAY define.
 *                      Added MPI2_EVENT_SAS_DISC_DS_DOWNSTREAM_INITIATOR
 *                      define.
 *                      Added MPI2_EVENT_SAS_DEV_STAT_RC_SATA_INIT_FAILURE
 *                      define.
 *                      Removed MPI2_EVENT_SAS_DISC_DS_SATA_INIT_FAILURE define.
 *  05-06-09  02.00.11  Added MPI2_IOCFACTS_CAPABILITY_RAID_ACCELERATOR define.
 *                      Added MPI2_IOCFACTS_CAPABILITY_MSI_X_INDEX define.
 *                      Added two new reason codes for SAS Device Status Change
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 *                      Event.
 *                      Added new event: SAS PHY Counter.
 *  07-30-09  02.00.12  Added GPIO Interrupt event define and structure.
 *                      Added MPI2_IOCFACTS_CAPABILITY_EXTENDED_BUFFER define.
 *                      Added new product id family for 2208.
 *  10-28-09  02.00.13  Added HostMSIxVectors field to MPI2_IOC_INIT_REQUEST.
 *                      Added MaxMSIxVectors field to MPI2_IOC_FACTS_REPLY.
 *                      Added MinDevHandle field to MPI2_IOC_FACTS_REPLY.
 *                      Added MPI2_IOCFACTS_CAPABILITY_HOST_BASED_DISCOVERY.
 *                      Added MPI2_EVENT_HOST_BASED_DISCOVERY_PHY define.
 *                      Added MPI2_EVENT_SAS_TOPO_ES_NO_EXPANDER define.
 *                      Added Host Based Discovery Phy Event data.
 *                      Added defines for ProductID Product field
 *                      (MPI2_FW_HEADER_PID_).
 *                      Modified values for SAS ProductID Family
 *                      (MPI2_FW_HEADER_PID_FAMILY_).
 *  02-10-10  02.00.14  Added SAS Quiesce Event structure and defines.
 *                      Added PowerManagementControl Request structures and
 *                      defines.
 *  05-12-10  02.00.15  Marked Task Set Full Event as obsolete.
 *                      Added MPI2_EVENT_SAS_TOPO_LR_UNSUPPORTED_PHY define.
 *  11-10-10  02.00.16  Added MPI2_FW_DOWNLOAD_ITYPE_MIN_PRODUCT_SPECIFIC.
 *  02-23-11  02.00.17  Added SAS NOTIFY Primitive event, and added
 *                      SASNotifyPrimitiveMasks field to
 *                      MPI2_EVENT_NOTIFICATION_REQUEST.
 *                      Added Temperature Threshold Event.
 *                      Added Host Message Event.
 *                      Added Send Host Message request and reply.
 *  05-25-11  02.00.18  For Extended Image Header, added
 *                      MPI2_EXT_IMAGE_TYPE_MIN_PRODUCT_SPECIFIC and
 *                      MPI2_EXT_IMAGE_TYPE_MAX_PRODUCT_SPECIFIC defines.
 *                      Deprecated MPI2_EXT_IMAGE_TYPE_MAX define.
 *  08-24-11  02.00.19  Added PhysicalPort field to
 *                      MPI2_EVENT_DATA_SAS_DEVICE_STATUS_CHANGE structure.
 *                      Marked MPI2_PM_CONTROL_FEATURE_PCIE_LINK as obsolete.
 *  11-18-11  02.00.20  Incorporating additions for MPI v2.5.
 *  03-29-12  02.00.21  Added a product specific range to event values.
 *  07-26-12  02.00.22  Added MPI2_IOCFACTS_EXCEPT_PARTIAL_MEMORY_FAILURE.
 *                      Added ElapsedSeconds field to
 *                      MPI2_EVENT_DATA_IR_OPERATION_STATUS.
 *  08-19-13  02.00.23  For IOCInit, added MPI2_IOCINIT_MSGFLAG_RDPQ_ARRAY_MODE
 *                      and MPI2_IOC_INIT_RDPQ_ARRAY_ENTRY.
 *                      Added MPI2_IOCFACTS_CAPABILITY_RDPQ_ARRAY_CAPABLE.
 *                      Added MPI2_FW_DOWNLOAD_ITYPE_PUBLIC_KEY.
 *                      Added Encrypted Hash Extended Image.
 *  12-05-13  02.00.24  Added MPI25_HASH_IMAGE_TYPE_BIOS.
 *  --------------------------------------------------------------------------

mpi2_raid.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  08-31-07  02.00.01  Modifications to RAID Action request and reply,
 *                      including the Actions and ActionData.
 *  02-29-08  02.00.02  Added MPI2_RAID_ACTION_ADATA_DISABL_FULL_REBUILD.
 *  05-21-08  02.00.03  Added MPI2_RAID_VOL_CREATION_NUM_PHYSDISKS so that
 *                      the PhysDisk array in MPI2_RAID_VOLUME_CREATION_STRUCT
 *                      can be sized by the build environment.
 *  07-30-09  02.00.04  Added proper define for the Use Default Settings bit of
 *                      VolumeCreationFlags and marked the old one as obsolete.
 *  05-12-10  02.00.05  Added MPI2_RAID_VOL_FLAGS_OP_MDC define.
 *  08-24-10  02.00.06  Added MPI2_RAID_ACTION_COMPATIBILITY_CHECK along with
 *                      related structures and defines.
 *                      Added product-specific range to RAID Action values.
 *  11-18-11  02.00.07  Incorporating additions for MPI v2.5.
 *  02-06-12  02.00.08  Added MPI2_RAID_ACTION_PHYSDISK_HIDDEN.
 *  07-26-12  02.00.09  Added ElapsedSeconds field to MPI2_RAID_VOL_INDICATOR.
 *                      Added MPI2_RAID_VOL_FLAGS_ELAPSED_SECONDS_VALID define.
```



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 *  04-17-13  02.00.10  Added MPI25_RAID_ACTION_ADATA_ALLOW_PI.
 *  --------------------------------------------------------------------------

mpi2_sas.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-26-07  02.00.01  Added Clear All Persistent Operation to SAS IO Unit
 *                      Control Request.
 *  10-02-08  02.00.02  Added Set IOC Parameter Operation to SAS IO Unit Control
 *                      Request.
 *  10-28-09  02.00.03  Changed the type of SGL in MPI2_SATA_PASSTHROUGH_REQUEST
 *                      to MPI2_SGE_IO_UNION since it supports chained SGLs.
 *  05-12-10  02.00.04  Modified some comments.
 *  08-11-10  02.00.05  Added NCQ operations to SAS IO Unit Control.
 *  11-18-11  02.00.06  Incorporating additions for MPI v2.5.
 *  07-10-12  02.00.07  Added MPI2_SATA_PT_SGE_UNION for use in the SATA
 *                      Passthrough Request message.
 *  08-19-13  02.00.08  Made MPI2_SAS_OP_TRANSMIT_PORT_SELECT_SIGNAL obsolete
 *                      for anything newer than MPI v2.0.
 *  --------------------------------------------------------------------------

mpi2_targ.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  08-31-07  02.00.01  Added Command Buffer Data Location Address Space bits to
 *                      BufferPostFlags field of CommandBufferPostBase Request.
 *  02-29-08  02.00.02  Modified various names to make them 32-character unique.
 *  10-02-08  02.00.03  Removed NextCmdBufferOffset from
 *                      MPI2_TARGET_CMD_BUF_POST_BASE_REQUEST.
 *                      Target Status Send Request only takes a single SGE for
 *                      response data.
 *  02-10-10  02.00.04  Added comment to MPI2_TARGET_SSP_RSP_IU structure.
 *  11-18-11  02.00.05  Incorporating additions for MPI v2.5.
 *  11-27-12  02.00.06  Added InitiatorDevHandle field to MPI2_TARGET_MODE_ABORT
 *                      request message structure.
 *                      Added AbortType MPI2_TARGET_MODE_ABORT_DEVHANDLE and
 *                      MPI2_TARGET_MODE_ABORT_ALL_COMMANDS.
 *  --------------------------------------------------------------------------

mpi2_tool.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  12-18-07  02.00.01  Added Diagnostic Buffer Post and Diagnostic Release
 *                      structures and defines.
 *  02-29-08  02.00.02  Modified various names to make them 32-character unique.
 *  05-06-09  02.00.03  Added ISTWI Read Write Tool and Diagnostic CLI Tool.
 *  07-30-09  02.00.04  Added ExtendedType field to DiagnosticBufferPost request
 *                      and reply messages.
 *                      Added MPI2_DIAG_BUF_TYPE_EXTENDED.
 *                      Incremented MPI2_DIAG_BUF_TYPE_COUNT.
 *  05-12-10  02.00.05  Added Diagnostic Data Upload tool.
 *  08-11-10  02.00.06  Added defines that were missing for Diagnostic Buffer
 *                      Post Request.
 *  05-25-11  02.00.07  Added Flags field and related defines to
 *                      MPI2_TOOLBOX_ISTWI_READ_WRITE_REQUEST.
 *  11-18-11  02.00.08  Incorporating additions for MPI v2.5.
 *  07-10-12  02.00.09  Add MPI v2.5 Toolbox Diagnostic CLI Tool Request
 *                      message.
 *  07-26-12  02.00.10  Modified MPI2_TOOLBOX_DIAGNOSTIC_CLI_REQUEST so that
 *                      it uses MPI Chain SGE as well as MPI Simple SGE.
 *  08-19-13  02.00.11  Added MPI2_TOOLBOX_TEXT_DISPLAY_TOOL and related info.
 *  --------------------------------------------------------------------------

mpi2_type.h
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  --------------------------------------------------------------------------

mpi2_ra.h
 *  05-06-09  02.00.00  Initial version.
```

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 *  --------------------------------------------------------------------------

mpi2_hbd.h
 *  10-28-09  02.00.00  Initial version.
 *  08-11-10  02.00.01  Removed PortGroups, DmaGroup, and ControlGroup from
 *                      HBD Action request, replaced by AdditionalInfo field.
 *  11-18-11  02.00.02  Incorporating additions for MPI v2.5.
 *  --------------------------------------------------------------------------


mpi2_history.txt         Parts list history

Filename     02.00.33  02.00.32  02.00.31  02.00.30
----------   --------  --------  --------  --------
mpi2.h       02.00.33  02.00.32  02.00.31  02.00.30
mpi2_cnfg.h  02.00.27  02.00.26  02.00.25  02.00.25
mpi2_init.h  02.00.15  02.00.15  02.00.15  02.00.15
mpi2_ioc.h   02.00.24  02.00.23  02.00.22  02.00.22
mpi2_raid.h  02.00.10  02.00.10  02.00.10  02.00.09
mpi2_sas.h   02.00.08  02.00.08  02.00.07  02.00.07
mpi2_targ.h  02.00.06  02.00.06  02.00.06  02.00.06
mpi2_tool.h  02.00.11  02.00.11  02.00.10  02.00.10
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_ra.h    02.00.00  02.00.00  02.00.00  02.00.00
mpi2_hbd.h   02.00.02  02.00.02  02.00.02  02.00.02

Filename     02.00.29  02.00.28  02.00.27  02.00.26  02.00.25  02.00.24
----------   --------  --------  --------  --------  --------  --------
mpi2.h       02.00.29  02.00.28  02.00.27  02.00.26  02.00.25  02.00.24
mpi2_cnfg.h  02.00.24  02.00.23  02.00.22  02.00.22  02.00.22  02.00.22
mpi2_init.h  02.00.14  02.00.14  02.00.14  02.00.14  02.00.13  02.00.13
mpi2_ioc.h   02.00.22  02.00.22  02.00.22  02.00.21  02.00.21  02.00.20
mpi2_raid.h  02.00.09  02.00.09  02.00.09  02.00.08  02.00.08  02.00.08
mpi2_sas.h   02.00.07  02.00.07  02.00.07  02.00.07  02.00.06  02.00.06
mpi2_targ.h  02.00.06  02.00.06  02.00.05  02.00.05  02.00.05  02.00.05
mpi2_tool.h  02.00.10  02.00.10  02.00.10  02.00.09  02.00.08  02.00.08
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_ra.h    02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_hbd.h   02.00.02  02.00.02  02.00.02  02.00.02  02.00.02  02.00.02

Filename     02.00.23  02.00.22  02.00.21  02.00.20  02.00.19  02.00.18
----------   --------  --------  --------  --------  --------  --------
mpi2.h       02.00.23  02.00.22  02.00.21  02.00.20  02.00.19  02.00.18
mpi2_cnfg.h  02.00.22  02.00.21  02.00.20  02.00.19  02.00.18  02.00.17
mpi2_init.h  02.00.12  02.00.11  02.00.11  02.00.11  02.00.11  02.00.11
mpi2_ioc.h   02.00.20  02.00.19  02.00.18  02.00.17  02.00.17  02.00.16
mpi2_raid.h  02.00.07  02.00.06  02.00.05  02.00.05  02.00.05  02.00.05
mpi2_sas.h   02.00.06  02.00.05  02.00.05  02.00.05  02.00.05  02.00.05
mpi2_targ.h  02.00.05  02.00.04  02.00.04  02.00.04  02.00.04  02.00.04
mpi2_tool.h  02.00.08  02.00.07  02.00.07  02.00.06  02.00.06  02.00.06
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_ra.h    02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_hbd.h   02.00.02  02.00.01  02.00.01  02.00.01  02.00.01  02.00.01

Filename     02.00.17  02.00.16  02.00.15  02.00.14  02.00.13  02.00.12
----------   --------  --------  --------  --------  --------  --------
mpi2.h       02.00.17  02.00.16  02.00.15  02.00.14  02.00.13  02.00.12
mpi2_cnfg.h  02.00.16  02.00.15  02.00.14  02.00.13  02.00.12  02.00.11
mpi2_init.h  02.00.10  02.00.10  02.00.09  02.00.08  02.00.07  02.00.07
mpi2_ioc.h   02.00.15  02.00.15  02.00.14  02.00.13  02.00.12  02.00.11
mpi2_raid.h  02.00.05  02.00.05  02.00.04  02.00.04  02.00.04  02.00.03
mpi2_sas.h   02.00.05  02.00.04  02.00.03  02.00.03  02.00.02  02.00.02
mpi2_targ.h  02.00.04  02.00.04  02.00.04  02.00.03  02.00.03  02.00.03
mpi2_tool.h  02.00.06  02.00.05  02.00.04  02.00.04  02.00.04  02.00.03
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_ra.h    02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
```



```
mpi2_hbd.h   02.00.01  02.00.00  02.00.00  02.00.00

Filename     02.00.11  02.00.10  02.00.09  02.00.08  02.00.07  02.00.06
----------   --------  --------  --------  --------  --------  --------
mpi2.h       02.00.11  02.00.10  02.00.09  02.00.08  02.00.07  02.00.06
mpi2_cnfg.h  02.00.10  02.00.09  02.00.08  02.00.07  02.00.06  02.00.06
mpi2_init.h  02.00.06  02.00.06  02.00.05  02.00.05  02.00.04  02.00.03
mpi2_ioc.h   02.00.10  02.00.09  02.00.08  02.00.07  02.00.07  02.00.06
mpi2_raid.h  02.00.03  02.00.03  02.00.03  02.00.03  02.00.02  02.00.02
mpi2_sas.h   02.00.02  02.00.02  02.00.01  02.00.01  02.00.01  02.00.01
mpi2_targ.h  02.00.03  02.00.03  02.00.02  02.00.02  02.00.02  02.00.02
mpi2_tool.h  02.00.02  02.00.02  02.00.02  02.00.02  02.00.02  02.00.02
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00

Filename     02.00.05  02.00.04  02.00.03  02.00.02  02.00.01  02.00.00
----------   --------  --------  --------  --------  --------  --------
mpi2.h       02.00.05  02.00.04  02.00.03  02.00.02  02.00.01  02.00.00
mpi2_cnfg.h  02.00.05  02.00.04  02.00.03  02.00.02  02.00.01  02.00.00
mpi2_init.h  02.00.02  02.00.01  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_ioc.h   02.00.05  02.00.04  02.00.03  02.00.02  02.00.01  02.00.00
mpi2_raid.h  02.00.01  02.00.01  02.00.01  02.00.00  02.00.00  02.00.00
mpi2_sas.h   02.00.01  02.00.01  02.00.01  02.00.01  02.00.00  02.00.00
mpi2_targ.h  02.00.01  02.00.01  02.00.01  02.00.00  02.00.00  02.00.00
mpi2_tool.h  02.00.01  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
mpi2_type.h  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00  02.00.00
```

```
**********************************************************
   30283 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_init.h
NEX-1888 upstream
**********************************************************
```

```
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 * DAMAGE.
 */

/*
 *          Name:  mpi2_init.h
 *         Title:  MPI SCSI initiator mode messages and structures
 *  Creation Date:  June 23, 2006
 *
 *  mpi2_init.h Version:  02.00.15
 *    mpi2_init.h Version:  02.00.07
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  10-31-07  02.00.01  Fixed name for pMpi2SCSITaskManagementRequest_t.
 *  12-18-07  02.00.02  Modified Task Management Target Reset Method defines.
 *  02-29-08  02.00.03  Added Query Task Set and Query Unit Attention.
 *  03-03-08  02.00.04  Fixed name of struct _MPI2_SCSI_TASK_MANAGE_REPLY.
 *  05-21-08  02.00.05  Fixed typo in name of Mpi2SepRequest_t.
 *  10-02-08  02.00.06  Removed Untagged and No Disconnect values from SCSI IO
 *                      Control field Task Attribute flags.
 *                      Moved LUN field defines to mpi2.h becasue they are
 *                      common to many structures.
 *  05-06-09  02.00.07  Changed task management type of Query Unit Attention to
 *                      Query Asynchronous Event.
 *                      Defined two new bits in the SlotStatus field of the SCSI
 *                      Enclosure Processor Request and Reply.
 *  10-28-09  02.00.08  Added defines for decoding the ResponseInfo bytes for
 *                      both SCSI IO Error Reply and SCSI Task Management Reply.
 *                      Added ResponseInfo field to MPI2_SCSI_TASK_MANAGE_REPLY.
 *                      Added MPI2_SCSITASKMGMT_RSP_TM_OVERLAPPED_TAG define.
 *  02-10-10  02.00.09  Removed unused structure that had "#if 0" around it.
 *  05-12-10  02.00.10  Added optional vendor-unique region to SCSI IO Request.
 *  11-10-10  02.00.11  Added MPI2_SCSIIO_NUM_SGLOFFSETS define.
 *  11-18-11  02.00.12  Incorporating additions for MPI v2.5.
 *  02-06-12  02.00.13  Added alternate defines for Task Priority / Command
 *                      Priority to match SAM-4.
 *                      Added EEDPErrorOffset to MPI2_SCSI_IO_REPLY.
 *  07-10-12  02.00.14  Added MPI2_SCSIIO_CONTROL_SHIFT_DATADIRECTION.
 *  04-09-13  02.00.15  Added SCSIStatusQualifier field to MPI2_SCSI_IO_REPLY,
 *                      replacing the Reserved4 field.
 *  ---------------------------------------------------------------------------
 */

#ifndef MPI2_INIT_H
#define MPI2_INIT_H

/*****************************************************************************
```

```
 85 *
 86 *               SCSI Initiator Messages
 87 *
 88 ****************************************************************************/

 90 /****************************************************************************
 91 *  SCSI IO messages and associated structures
 92 ****************************************************************************/

 94 typedef struct _MPI2_SCSI_IO_CDB_EEDP32
 91 typedef struct
 95 {
 96     U8                      CDB[20];                    /* 0x00 */
 97     U32                     PrimaryReferenceTag;        /* 0x14 */
 98     U16                     PrimaryApplicationTag;      /* 0x18 */
 99     U16                     PrimaryApplicationTagMask;  /* 0x1A */
100     U32                     TransferLength;             /* 0x1C */
101 } MPI2_SCSI_IO_CDB_EEDP32, MPI2_POINTER PTR_MPI2_SCSI_IO_CDB_EEDP32,
102   Mpi2ScsiIoCdbEedp32_t, MPI2_POINTER pMpi2ScsiIoCdbEedp32_t;

104 /* MPI v2.0 CDB field */
105 typedef union _MPI2_SCSI_IO_CDB_UNION
101 /* TBD: I don't think this is needed for MPI2/Gen2 */
102 #if 0
103 typedef struct
106 {
105     U8                      CDB[16];                    /* 0x00 */
106     U32                     DataLength;                 /* 0x10 */
107     U32                     PrimaryReferenceTag;        /* 0x14 */
108     U16                     PrimaryApplicationTag;      /* 0x18 */
109     U16                     PrimaryApplicationTagMask;  /* 0x1A */
110     U32                     TransferLength;             /* 0x1C */
111 } MPI2_SCSI_IO32_CDB_EEDP16, MPI2_POINTER PTR_MPI2_SCSI_IO32_CDB_EEDP16,
112   Mpi2ScsiIo32CdbEedp16_t, MPI2_POINTER pMpi2ScsiIo32CdbEedp16_t;
113 #endif

115 typedef union
116 {
107     U8                      CDB32[32];
108     MPI2_SCSI_IO_CDB_EEDP32 EEDP32;
109     MPI2_SGE_SIMPLE_UNION   SGE;
110 } MPI2_SCSI_IO_CDB_UNION, MPI2_POINTER PTR_MPI2_SCSI_IO_CDB_UNION,
111   Mpi2ScsiIoCdb_t, MPI2_POINTER pMpi2ScsiIoCdb_t;

113 /* MPI v2.0 SCSI IO Request Message */
123 /* SCSI IO Request Message */
114 typedef struct _MPI2_SCSI_IO_REQUEST
115 {
116     U16                     DevHandle;                  /* 0x00 */
117     U8                      ChainOffset;                /* 0x02 */
118     U8                      Function;                   /* 0x03 */
119     U16                     Reserved1;                  /* 0x04 */
120     U8                      Reserved2;                  /* 0x06 */
121     U8                      MsgFlags;                   /* 0x07 */
122     U8                      VP_ID;                      /* 0x08 */
123     U8                      VF_ID;                      /* 0x09 */
124     U16                     Reserved3;                  /* 0x0A */
125     U32                     SenseBufferLowAddress;      /* 0x0C */
126     U16                     SGLFlags;                   /* 0x10 */
127     U8                      SenseBufferLength;          /* 0x12 */
128     U8                      Reserved4;                  /* 0x13 */
129     U8                      SGLOffset0;                 /* 0x14 */
130     U8                      SGLOffset1;                 /* 0x15 */
131     U8                      SGLOffset2;                 /* 0x16 */
132     U8                      SGLOffset3;                 /* 0x17 */
133     U32                     SkipCount;                  /* 0x18 */
```



```
134     U32                     DataLength;                 /* 0x1C */
135     U32                     BidirectionalDataLength;    /* 0x20 */
136     U16                     IoFlags;                    /* 0x24 */
137     U16                     EEDPFlags;                  /* 0x26 */
138     U32                     EEDPBlockSize;              /* 0x28 */
139     U32                     SecondaryReferenceTag;      /* 0x2C */
140     U16                     SecondaryApplicationTag;    /* 0x30 */
141     U16                     ApplicationTagTranslationMask;  /* 0x32 */
142     U8                      LUN[8];                     /* 0x34 */
143     U32                     Control;                    /* 0x3C */
144     MPI2_SCSI_IO_CDB_UNION  CDB;                        /* 0x40 */

146 #ifdef MPI2_SCSI_IO_VENDOR_UNIQUE_REGION /* typically this is left undefined */
147     MPI2_SCSI_IO_VENDOR_UNIQUE VendorRegion;
148 #endif

150     MPI2_SGE_IO_UNION       SGL;                        /* 0x60 */

152 } MPI2_SCSI_IO_REQUEST, MPI2_POINTER PTR_MPI2_SCSI_IO_REQUEST,
153   Mpi2SCSIIORequest_t, MPI2_POINTER pMpi2SCSIIORequest_t;

155 /* SCSI IO MsgFlags bits */

157 /* MsgFlags for SenseBufferAddressSpace */
158 #define MPI2_SCSIIO_MSGFLAGS_MASK_SENSE_ADDR        (0x0C)
159 #define MPI2_SCSIIO_MSGFLAGS_SYSTEM_SENSE_ADDR      (0x00)
160 #define MPI2_SCSIIO_MSGFLAGS_IOCDDR_SENSE_ADDR      (0x04)
161 #define MPI2_SCSIIO_MSGFLAGS_IOCPLB_SENSE_ADDR      (0x08)
162 #define MPI2_SCSIIO_MSGFLAGS_IOCPLBNTA_SENSE_ADDR   (0x0C)

164 /* SCSI IO SGLFlags bits */

166 /* base values for Data Location Address Space */
167 #define MPI2_SCSIIO_SGLFLAGS_ADDR_MASK              (0x0C)
168 #define MPI2_SCSIIO_SGLFLAGS_SYSTEM_ADDR            (0x00)
169 #define MPI2_SCSIIO_SGLFLAGS_IOCDDR_ADDR            (0x04)
170 #define MPI2_SCSIIO_SGLFLAGS_IOCPLB_ADDR            (0x08)
171 #define MPI2_SCSIIO_SGLFLAGS_IOCPLBNTA_ADDR         (0x0C)

173 /* base values for Type */
174 #define MPI2_SCSIIO_SGLFLAGS_TYPE_MASK              (0x03)
175 #define MPI2_SCSIIO_SGLFLAGS_TYPE_MPI               (0x00)
176 #define MPI2_SCSIIO_SGLFLAGS_TYPE_IEEE32            (0x01)
177 #define MPI2_SCSIIO_SGLFLAGS_TYPE_IEEE64            (0x02)

179 /* shift values for each sub-field */
180 #define MPI2_SCSIIO_SGLFLAGS_SGL3_SHIFT             (12)
181 #define MPI2_SCSIIO_SGLFLAGS_SGL2_SHIFT             (8)
182 #define MPI2_SCSIIO_SGLFLAGS_SGL1_SHIFT             (4)
183 #define MPI2_SCSIIO_SGLFLAGS_SGL0_SHIFT             (0)

185 /* number of SGLOffset fields */
186 #define MPI2_SCSIIO_NUM_SGLOFFSETS                  (4)

188 /* SCSI IO IoFlags bits */

190 /* Large CDB Address Space */
191 #define MPI2_SCSIIO_CDB_ADDR_MASK                   (0x6000)
192 #define MPI2_SCSIIO_CDB_ADDR_SYSTEM                 (0x0000)
193 #define MPI2_SCSIIO_CDB_ADDR_IOCDDR                 (0x2000)
194 #define MPI2_SCSIIO_CDB_ADDR_IOCPLB                 (0x4000)
195 #define MPI2_SCSIIO_CDB_ADDR_IOCPLBNTA              (0x6000)

197 #define MPI2_SCSIIO_IOFLAGS_LARGE_CDB               (0x1000)
198 #define MPI2_SCSIIO_IOFLAGS_BIDIRECTIONAL           (0x0800)
199 #define MPI2_SCSIIO_IOFLAGS_MULTICAST               (0x0400)
```

```
200 #define MPI2_SCSIIO_IOFLAGS_CMD_DETERMINES_DATA_DIR (0x0200)
201 #define MPI2_SCSIIO_IOFLAGS_CDBLENGTH_MASK          (0x01FF)

203 /* SCSI IO EEDPFlags bits */

205 #define MPI2_SCSIIO_EEDPFLAGS_INC_PRI_REFTAG        (0x8000)
206 #define MPI2_SCSIIO_EEDPFLAGS_INC_SEC_REFTAG        (0x4000)
207 #define MPI2_SCSIIO_EEDPFLAGS_INC_PRI_APPTAG        (0x2000)
208 #define MPI2_SCSIIO_EEDPFLAGS_INC_SEC_APPTAG        (0x1000)

210 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_REFTAG          (0x0400)
211 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_APPTAG          (0x0200)
212 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_GUARD           (0x0100)

214 #define MPI2_SCSIIO_EEDPFLAGS_PASSTHRU_REFTAG       (0x0008)

216 #define MPI2_SCSIIO_EEDPFLAGS_MASK_OP               (0x0007)
217 #define MPI2_SCSIIO_EEDPFLAGS_NOOP_OP               (0x0000)
218 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_OP              (0x0001)
219 #define MPI2_SCSIIO_EEDPFLAGS_STRIP_OP              (0x0002)
220 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_REMOVE_OP       (0x0003)
221 #define MPI2_SCSIIO_EEDPFLAGS_INSERT_OP             (0x0004)
222 #define MPI2_SCSIIO_EEDPFLAGS_REPLACE_OP            (0x0006)
223 #define MPI2_SCSIIO_EEDPFLAGS_CHECK_REGEN_OP        (0x0007)

225 /* SCSI IO LUN fields: use MPI2_LUN_ from mpi2.h */

227 /* SCSI IO Control bits */
228 #define MPI2_SCSIIO_CONTROL_ADDCDBLEN_MASK      (0xFC000000)
229 #define MPI2_SCSIIO_CONTROL_ADDCDBLEN_SHIFT     (26)

231 #define MPI2_SCSIIO_CONTROL_DATADIRECTION_MASK  (0x03000000)
232 #define MPI2_SCSIIO_CONTROL_SHIFT_DATADIRECTION (24)
233 #define MPI2_SCSIIO_CONTROL_NODATATRANSFER      (0x00000000)
234 #define MPI2_SCSIIO_CONTROL_WRITE               (0x01000000)
235 #define MPI2_SCSIIO_CONTROL_READ                (0x02000000)
236 #define MPI2_SCSIIO_CONTROL_BIDIRECTIONAL       (0x03000000)

238 #define MPI2_SCSIIO_CONTROL_TASKPRI_MASK        (0x00007800)
239 #define MPI2_SCSIIO_CONTROL_TASKPRI_SHIFT       (11)
240 /* alternate name for the previous field; called Command Priority in SAM-4 */
241 #define MPI2_SCSIIO_CONTROL_CMDPRI_MASK         (0x00007800)
242 #define MPI2_SCSIIO_CONTROL_CMDPRI_SHIFT        (11)

244 #define MPI2_SCSIIO_CONTROL_TASKATTRIBUTE_MASK  (0x00000700)
245 #define MPI2_SCSIIO_CONTROL_SIMPLEQ             (0x00000000)
246 #define MPI2_SCSIIO_CONTROL_HEADOFQ             (0x00000100)
247 #define MPI2_SCSIIO_CONTROL_ORDEREDQ            (0x00000200)
248 #define MPI2_SCSIIO_CONTROL_ACAQ                (0x00000400)

250 #define MPI2_SCSIIO_CONTROL_TLR_MASK            (0x000000C0)
251 #define MPI2_SCSIIO_CONTROL_NO_TLR              (0x00000000)
252 #define MPI2_SCSIIO_CONTROL_TLR_ON              (0x00000040)
253 #define MPI2_SCSIIO_CONTROL_TLR_OFF             (0x00000080)


256 /* MPI v2.5 CDB field */
257 typedef union _MPI25_SCSI_IO_CDB_UNION
258 {
259     U8                      CDB32[32];
260     MPI2_SCSI_IO_CDB_EEDP32 EEDP32;
261     MPI2_IEEE_SGE_SIMPLE64  SGE;
262 } MPI25_SCSI_IO_CDB_UNION, MPI2_POINTER PTR_MPI25_SCSI_IO_CDB_UNION,
263   Mpi25ScsiIoCdb_t, MPI2_POINTER pMpi25ScsiIoCdb_t;

265 /* MPI v2.5 SCSI IO Request Message */
```



```
266 typedef struct _MPI25_SCSI_IO_REQUEST
267 {
268     U16                     DevHandle;                  /* 0x00 */
269     U8                      ChainOffset;                /* 0x02 */
270     U8                      Function;                   /* 0x03 */
271     U16                     Reserved1;                  /* 0x04 */
272     U8                      Reserved2;                  /* 0x06 */
273     U8                      MsgFlags;                   /* 0x07 */
274     U8                      VP_ID;                      /* 0x08 */
275     U8                      VF_ID;                      /* 0x09 */
276     U16                     Reserved3;                  /* 0x0A */
277     U32                     SenseBufferLowAddress;      /* 0x0C */
278     U8                      DMAFlags;                   /* 0x10 */
279     U8                      Reserved5;                  /* 0x11 */
280     U8                      SenseBufferLength;          /* 0x12 */
281     U8                      Reserved4;                  /* 0x13 */
282     U8                      SGLOffset0;                 /* 0x14 */
283     U8                      SGLOffset1;                 /* 0x15 */
284     U8                      SGLOffset2;                 /* 0x16 */
285     U8                      SGLOffset3;                 /* 0x17 */
286     U32                     SkipCount;                  /* 0x18 */
287     U32                     DataLength;                 /* 0x1C */
288     U32                     BidirectionalDataLength;    /* 0x20 */
289     U16                     IoFlags;                    /* 0x24 */
290     U16                     EEDPFlags;                  /* 0x26 */
291     U16                     EEDPBlockSize;              /* 0x28 */
292     U16                     Reserved6;                  /* 0x2A */
293     U32                     SecondaryReferenceTag;      /* 0x2C */
294     U16                     SecondaryApplicationTag;    /* 0x30 */
295     U16                     ApplicationTagTranslationMask; /* 0x32 */
296     U8                      LUN[8];                     /* 0x34 */
297     U32                     Control;                    /* 0x3C */
298     MPI25_SCSI_IO_CDB_UNION CDB;                        /* 0x40 */

300 #ifdef MPI25_SCSI_IO_VENDOR_UNIQUE_REGION /* typically this is left undefined */
301     MPI25_SCSI_IO_VENDOR_UNIQUE VendorRegion;
302 #endif

304     MPI25_SGE_IO_UNION      SGL;                        /* 0x60 */

306 } MPI25_SCSI_IO_REQUEST, MPI2_POINTER PTR_MPI25_SCSI_IO_REQUEST,
307   Mpi25SCSIIORequest_t, MPI2_POINTER pMpi25SCSIIORequest_t;

309 /* use MPI2_SCSIIO_MSGFLAGS_ defines for the MsgFlags field */

311 /* Defines for the DMAFlags field
312  *  Each setting affects 4 SGLS, from SGL0 to SGL3.
313  *      D = Data
314  *      C = Cache DIF
315  *      I = Interleaved
316  *      H = Host DIF
317  */
318 #define MPI25_SCSIIO_DMAFLAGS_OP_MASK               (0x0F)
319 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_D_D            (0x00)
320 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_D_C            (0x01)
321 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_D_I            (0x02)
322 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_C_C            (0x03)
323 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_C_I            (0x04)
324 #define MPI25_SCSIIO_DMAFLAGS_OP_D_D_I_I            (0x05)
325 #define MPI25_SCSIIO_DMAFLAGS_OP_D_C_C_C            (0x06)
326 #define MPI25_SCSIIO_DMAFLAGS_OP_D_C_C_I            (0x07)
327 #define MPI25_SCSIIO_DMAFLAGS_OP_D_C_I_I            (0x08)
328 #define MPI25_SCSIIO_DMAFLAGS_OP_D_I_I_I            (0x09)
329 #define MPI25_SCSIIO_DMAFLAGS_OP_D_H_D_D            (0x0A)
330 #define MPI25_SCSIIO_DMAFLAGS_OP_D_H_D_C            (0x0B)
331 #define MPI25_SCSIIO_DMAFLAGS_OP_D_H_D_I            (0x0C)
```

```
#define MPI25_SCSIIO_DMAFLAGS_OP_D_H_C_C            (0x0D)
#define MPI25_SCSIIO_DMAFLAGS_OP_D_H_C_I            (0x0E)
#define MPI25_SCSIIO_DMAFLAGS_OP_D_H_I_I            (0x0F)

/* number of SGLOffset fields */
#define MPI25_SCSIIO_NUM_SGLOFFSETS                 (4)

/* defines for the IoFlags field */
#define MPI25_SCSIIO_IOFLAGS_IO_PATH_MASK           (0xC000)
#define MPI25_SCSIIO_IOFLAGS_NORMAL_PATH            (0x0000)
#define MPI25_SCSIIO_IOFLAGS_FAST_PATH              (0x4000)

#define MPI25_SCSIIO_IOFLAGS_LARGE_CDB                  (0x1000)
#define MPI25_SCSIIO_IOFLAGS_BIDIRECTIONAL              (0x0800)
#define MPI25_SCSIIO_IOFLAGS_CDBLENGTH_MASK             (0x01FF)

/* MPI v2.5 defines for the EEDPFlags bits */
/* use MPI2_SCSIIO_EEDPFLAGS_ defines for the other EEDPFlags bits */
#define MPI25_SCSIIO_EEDPFLAGS_ESCAPE_MODE_MASK             (0x00C0)
#define MPI25_SCSIIO_EEDPFLAGS_COMPATIBLE_MODE              (0x0000)
#define MPI25_SCSIIO_EEDPFLAGS_DO_NOT_DISABLE_MODE          (0x0040)
#define MPI25_SCSIIO_EEDPFLAGS_APPTAG_DISABLE_MODE          (0x0080)
#define MPI25_SCSIIO_EEDPFLAGS_APPTAG_REFTAG_DISABLE_MODE   (0x00C0)

#define MPI25_SCSIIO_EEDPFLAGS_HOST_GUARD_METHOD_MASK       (0x0030)
#define MPI25_SCSIIO_EEDPFLAGS_T10_CRC_HOST_GUARD           (0x0000)
#define MPI25_SCSIIO_EEDPFLAGS_IP_CHKSUM_HOST_GUARD         (0x0010)

/* use MPI2_LUN_ defines from mpi2.h for the LUN field */

/* use MPI2_SCSIIO_CONTROL_ defines for the Control field */


/* NOTE: The SCSI IO Reply is nearly the same for MPI 2.0 and MPI 2.5, so
 *       MPI2_SCSI_IO_REPLY is used for both.
 */

/* SCSI IO Error Reply Message */
typedef struct _MPI2_SCSI_IO_REPLY
{
    U16                     DevHandle;                  /* 0x00 */
    U8                      MsgLength;                  /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved1;                  /* 0x04 */
    U8                      Reserved2;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U8                      SCSIStatus;                 /* 0x0C */
    U8                      SCSIState;                  /* 0x0D */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
    U32                     TransferCount;              /* 0x14 */
    U32                     SenseCount;                 /* 0x18 */
    U32                     ResponseInfo;               /* 0x1C */
    U16                     TaskTag;                    /* 0x20 */
    U16                     SCSIStatusQualifier;        /* 0x22 */
    U16                     Reserved4;                  /* 0x22 */
    U32                     BidirectionalTransferCount; /* 0x24 */
    U32                     EEDPErrorOffset;            /* 0x28 */ /* MPI 2.
    U32                     Reserved5;                  /* 0x28 */
    U32                     Reserved6;                  /* 0x2C */
} MPI2_SCSI_IO_REPLY, MPI2_POINTER PTR_MPI2_SCSI_IO_REPLY,
  Mpi2SCSIIOReply_t, MPI2_POINTER pMpi2SCSIIOReply_t;
```



```
/* SCSI IO Reply SCSIStatus values (SAM-4 status codes) */

#define MPI2_SCSI_STATUS_GOOD                   (0x00)
#define MPI2_SCSI_STATUS_CHECK_CONDITION        (0x02)
#define MPI2_SCSI_STATUS_CONDITION_MET          (0x04)
#define MPI2_SCSI_STATUS_BUSY                   (0x08)
#define MPI2_SCSI_STATUS_INTERMEDIATE           (0x10)
#define MPI2_SCSI_STATUS_INTERMEDIATE_CONDMET   (0x14)
#define MPI2_SCSI_STATUS_RESERVATION_CONFLICT   (0x18)
#define MPI2_SCSI_STATUS_COMMAND_TERMINATED     (0x22) /* obsolete */
#define MPI2_SCSI_STATUS_TASK_SET_FULL          (0x28)
#define MPI2_SCSI_STATUS_ACA_ACTIVE             (0x30)
#define MPI2_SCSI_STATUS_TASK_ABORTED           (0x40)

/* SCSI IO Reply SCSIState flags */

#define MPI2_SCSI_STATE_RESPONSE_INFO_VALID     (0x10)
#define MPI2_SCSI_STATE_TERMINATED              (0x08)
#define MPI2_SCSI_STATE_NO_SCSI_STATUS          (0x04)
#define MPI2_SCSI_STATE_AUTOSENSE_FAILED        (0x02)
#define MPI2_SCSI_STATE_AUTOSENSE_VALID         (0x01)

/* masks and shifts for the ResponseInfo field */

#define MPI2_SCSI_RI_MASK_REASONCODE            (0x000000FF)
#define MPI2_SCSI_RI_SHIFT_REASONCODE           (0)

#define MPI2_SCSI_TASKTAG_UNKNOWN               (0xFFFF)


/*****************************************************************************
*  SCSI Task Management messages
*****************************************************************************/

/* SCSI Task Management Request Message */
typedef struct _MPI2_SCSI_TASK_MANAGE_REQUEST
{
    U16                     DevHandle;                  /* 0x00 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U8                      Reserved1;                  /* 0x04 */
    U8                      TaskType;                   /* 0x05 */
    U8                      Reserved2;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U8                      LUN[8];                     /* 0x0C */
    U32                     Reserved4[7];               /* 0x14 */
    U16                     TaskMID;                    /* 0x30 */
    U16                     Reserved5;                  /* 0x32 */
} MPI2_SCSI_TASK_MANAGE_REQUEST,
  MPI2_POINTER PTR_MPI2_SCSI_TASK_MANAGE_REQUEST,
  Mpi2SCSITaskManagementRequest_t,
  MPI2_POINTER pMpi2SCSITaskManagementRequest_t;

/* TaskType values */

#define MPI2_SCSITASKMGMT_TASKTYPE_ABORT_TASK           (0x01)
#define MPI2_SCSITASKMGMT_TASKTYPE_ABRT_TASK_SET        (0x02)
#define MPI2_SCSITASKMGMT_TASKTYPE_TARGET_RESET         (0x03)
#define MPI2_SCSITASKMGMT_TASKTYPE_LOGICAL_UNIT_RESET   (0x05)
#define MPI2_SCSITASKMGMT_TASKTYPE_CLEAR_TASK_SET       (0x06)
#define MPI2_SCSITASKMGMT_TASKTYPE_QUERY_TASK           (0x07)
#define MPI2_SCSITASKMGMT_TASKTYPE_CLR_ACA              (0x08)
#define MPI2_SCSITASKMGMT_TASKTYPE_QRY_TASK_SET         (0x09)
```

```
462 #define MPI2_SCSITASKMGMT_TASKTYPE_QRY_ASYNC_EVENT      (0x0A)

464 /* obsolete TaskType name */
465 #define MPI2_SCSITASKMGMT_TASKTYPE_QRY_UNIT_ATTENTION   (MPI2_SCSITASKMGMT_TASKT

467 /* MsgFlags bits */

469 #define MPI2_SCSITASKMGMT_MSGFLAGS_MASK_TARGET_RESET    (0x18)
470 #define MPI2_SCSITASKMGMT_MSGFLAGS_LINK_RESET           (0x00)
471 #define MPI2_SCSITASKMGMT_MSGFLAGS_NEXUS_RESET_SRST     (0x08)
472 #define MPI2_SCSITASKMGMT_MSGFLAGS_SAS_HARD_LINK_RESET  (0x10)

474 #define MPI2_SCSITASKMGMT_MSGFLAGS_DO_NOT_SEND_TASK_IU  (0x01)



478 /* SCSI Task Management Reply Message */
479 typedef struct _MPI2_SCSI_TASK_MANAGE_REPLY
480 {
481     U16                     DevHandle;                  /* 0x00 */
482     U8                      MsgLength;                  /* 0x02 */
483     U8                      Function;                   /* 0x03 */
484     U8                      ResponseCode;               /* 0x04 */
485     U8                      TaskType;                   /* 0x05 */
486     U8                      Reserved1;                  /* 0x06 */
487     U8                      MsgFlags;                   /* 0x07 */
488     U8                      VP_ID;                      /* 0x08 */
489     U8                      VF_ID;                      /* 0x09 */
490     U16                     Reserved2;                  /* 0x0A */
491     U16                     Reserved3;                  /* 0x0C */
492     U16                     IOCStatus;                  /* 0x0E */
493     U32                     IOCLogInfo;                 /* 0x10 */
494     U32                     TerminationCount;           /* 0x14 */
495     U32                     ResponseInfo;               /* 0x18 */
496 } MPI2_SCSI_TASK_MANAGE_REPLY,
497   MPI2_POINTER PTR_MPI2_SCSI_TASK_MANAGE_REPLY,
498   Mpi2SCSITaskManagementReply_t, MPI2_POINTER pMpi2SCSIManagementReply_t;

500 /* ResponseCode values */

502 #define MPI2_SCSITASKMGMT_RSP_TM_COMPLETE               (0x00)
503 #define MPI2_SCSITASKMGMT_RSP_INVALID_FRAME             (0x02)
504 #define MPI2_SCSITASKMGMT_RSP_TM_NOT_SUPPORTED          (0x04)
505 #define MPI2_SCSITASKMGMT_RSP_TM_FAILED                 (0x05)
506 #define MPI2_SCSITASKMGMT_RSP_TM_SUCCEEDED              (0x08)
507 #define MPI2_SCSITASKMGMT_RSP_TM_INVALID_LUN            (0x09)
508 #define MPI2_SCSITASKMGMT_RSP_TM_OVERLAPPED_TAG         (0x0A)
509 #define MPI2_SCSITASKMGMT_RSP_IO_QUEUED_ON_IOC          (0x80)

511 /* masks and shifts for the ResponseInfo field */

513 #define MPI2_SCSITASKMGMT_RI_MASK_REASONCODE            (0x000000FF)
514 #define MPI2_SCSITASKMGMT_RI_SHIFT_REASONCODE           (0)
515 #define MPI2_SCSITASKMGMT_RI_MASK_ARI2                  (0x0000FF00)
516 #define MPI2_SCSITASKMGMT_RI_SHIFT_ARI2                 (8)
517 #define MPI2_SCSITASKMGMT_RI_MASK_ARI1                  (0x00FF0000)
518 #define MPI2_SCSITASKMGMT_RI_SHIFT_ARI1                 (16)
519 #define MPI2_SCSITASKMGMT_RI_MASK_ARI0                  (0xFF000000)
520 #define MPI2_SCSITASKMGMT_RI_SHIFT_ARI0                 (24)


523 /*****************************************************************************
524 *  SCSI Enclosure Processor messages
525 *****************************************************************************/

527 /* SCSI Enclosure Processor Request Message */
```



```
528 typedef struct _MPI2_SEP_REQUEST
529 {
530     U16                     DevHandle;          /* 0x00 */
531     U8                      ChainOffset;        /* 0x02 */
532     U8                      Function;           /* 0x03 */
533     U8                      Action;             /* 0x04 */
534     U8                      Flags;              /* 0x05 */
535     U8                      Reserved1;          /* 0x06 */
536     U8                      MsgFlags;           /* 0x07 */
537     U8                      VP_ID;              /* 0x08 */
538     U8                      VF_ID;              /* 0x09 */
539     U16                     Reserved2;          /* 0x0A */
540     U32                     SlotStatus;         /* 0x0C */
541     U32                     Reserved3;          /* 0x10 */
542     U32                     Reserved4;          /* 0x14 */
543     U32                     Reserved5;          /* 0x18 */
544     U16                     Slot;               /* 0x1C */
545     U16                     EnclosureHandle;    /* 0x1E */
546 } MPI2_SEP_REQUEST, MPI2_POINTER PTR_MPI2_SEP_REQUEST,
______unchanged_portion_omitted_
```

```
**********************************************************
   94287 Tue Jun 17 10:46:18 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_ioc.h
NEX-1888 upstream
**********************************************************
```

```
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 * DAMAGE.
 */

/*
 *          Name:  mpi2_ioc.h
 *         Title:  MPI IOC, Port, Event, FW Download, and FW Upload messages
 *  Creation Date:  October 11, 2006
 *
 *  mpi2_ioc.h Version:  02.00.24
 *  mpi2_ioc.h Version:  02.00.12
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-04-07  02.00.01  In IOCFacts Reply structure, renamed MaxDevices to
 *                      MaxTargets.
 *                      Added TotalImageSize field to FWDownload Request.
 *                      Added reserved words to FWUpload Request.
 *  06-26-07  02.00.02  Added IR Configuration Change List Event.
 *  08-31-07  02.00.03  Removed SystemReplyQueueDepth field from the IOCInit
 *                      request and replaced it with
 *                      ReplyDescriptorPostQueueDepth and ReplyFreeQueueDepth.
 *                      Replaced the MinReplyQueueDepth field of the IOCFacts
 *                      reply with MaxReplyDescriptorPostQueueDepth.
 *                      Added MPI2_RDPQ_DEPTH_MIN define to specify the minimum
 *                      depth for the Reply Descriptor Post Queue.
 *                      Added SASAddress field to Initiator Device Table
 *                      Overflow Event data.
 *  10-31-07  02.00.04  Added ReasonCode MPI2_EVENT_SAS_INIT_RC_NOT_RESPONDING
 *                      for SAS Initiator Device Status Change Event data.
 *                      Modified Reason Code defines for SAS Topology Change
 *                      List Event data, including adding a bit for PHY Vacant
 *                      status, and adding a mask for the Reason Code.
 *                      Added define for
 *                      MPI2_EVENT_SAS_TOPO_ES_DELAY_NOT_RESPONDING.
 *                      Added define for MPI2_EXT_IMAGE_TYPE_MEGARAID.
 *  12-18-07  02.00.05  Added Boot Status defines for the IOCExceptions field of
 *                      the IOCFacts Reply.
 *                      Removed MPI2_IOCFACTS_CAPABILITY_EXTENDED_BUFFER define.
 *                      Moved MPI2_VERSION_UNION to mpi2.h.
 *                      Changed MPI2_EVENT_NOTIFICATION_REQUEST to use masks
 *                      instead of enables, and added SASBroadcastPrimitiveMasks
 *                      field.
 *                      Added Log Entry Added Event and related structure.
 *  02-29-08  02.00.06  Added define MPI2_IOCFACTS_CAPABILITY_INTEGRATED_RAID.
 *                      Removed define MPI2_IOCFACTS_PROTOCOL_SMP_TARGET.
 *                      Added MaxVolumes and MaxPersistentEntries fields to
 *                      IOCFacts reply.
```

```
 *                      Added ProtocalFlags and IOCCapabilities fields to
 *                      MPI2_FW_IMAGE_HEADER.
 *                      Removed MPI2_PORTENABLE_FLAGS_ENABLE_SINGLE_PORT.
 *  03-03-08  02.00.07  Fixed MPI2_FW_IMAGE_HEADER by changing Reserved26 to
 *                      a U16 (from a U32).
 *                      Removed extra 's' from EventMasks name.
 *  06-27-08  02.00.08  Fixed an offset in a comment.
 *  10-02-08  02.00.09  Removed SystemReplyFrameSize from MPI2_IOC_INIT_REQUEST.
 *                      Removed CurReplyFrameSize from MPI2_IOC_FACTS_REPLY and
 *                      renamed MinReplyFrameSize to ReplyFrameSize.
 *                      Added MPI2_IOCFACTS_EXCEPT_IR_FOREIGN_CONFIG_MAX.
 *                      Added two new RAIDOperation values for Integrated RAID
 *                      Operations Status Event data.
 *                      Added four new IR Configuration Change List Event data
 *                      ReasonCode values.
 *                      Added two new ReasonCode defines for SAS Device Status
 *                      Change Event data.
 *                      Added three new DiscoveryStatus bits for the SAS
 *                      Discovery event data.
 *                      Added Multiplexing Status Change bit to the PhyStatus
 *                      field of the SAS Topology Change List event data.
 *                      Removed define for MPI2_INIT_IMAGE_BOOTFLAGS_XMEMCOPY.
 *                      BootFlags are now product-specific.
 *                      Added defines for the indivdual signature bytes
 *                      for MPI2_INIT_IMAGE_FOOTER.
 *  01-19-09  02.00.10  Added MPI2_IOCFACTS_CAPABILITY_EVENT_REPLAY define.
 *                      Added MPI2_EVENT_SAS_DISC_DS_DOWNSTREAM_INITIATOR
 *                      define.
 *                      Added MPI2_EVENT_SAS_DEV_STAT_RC_SATA_INIT_FAILURE
 *                      define.
 *                      Removed MPI2_EVENT_SAS_DISC_DS_SATA_INIT_FAILURE define.
 *  05-06-09  02.00.11  Added MPI2_IOCFACTS_CAPABILITY_RAID_ACCELERATOR define.
 *                      Added MPI2_IOCFACTS_CAPABILITY_MSI_X_INDEX define.
 *                      Added two new reason codes for SAS Device Status Change
 *                      Event.
 *                      Added new event: SAS PHY Counter.
 *  07-30-09  02.00.12  Added GPIO Interrupt event define and structure.
 *                      Added MPI2_IOCFACTS_CAPABILITY_EXTENDED_BUFFER define.
 *                      Added new product id family for 2208.
 *  10-28-09  02.00.13  Added HostMSIxVectors field to MPI2_IOC_INIT_REQUEST.
 *                      Added MaxMSIxVectors field to MPI2_IOC_FACTS_REPLY.
 *                      Added MinDevHandle field to MPI2_IOC_FACTS_REPLY.
 *                      Added MPI2_IOCFACTS_CAPABILITY_HOST_BASED_DISCOVERY.
 *                      Added MPI2_EVENT_HOST_BASED_DISCOVERY_PHY define.
 *                      Added MPI2_EVENT_SAS_TOPO_ES_NO_EXPANDER define.
 *                      Added Host Based Discovery Phy Event data.
 *                      Added defines for ProductID Product field
 *                      (MPI2_FW_HEADER_PID_).
 *                      Modified values for SAS ProductID Family
 *                      (MPI2_FW_HEADER_PID_FAMILY_).
 *  02-10-10  02.00.14  Added SAS Quiesce Event structure and defines.
 *                      Added PowerManagementControl Request structures and
 *                      defines.
 *  05-12-10  02.00.15  Marked Task Set Full Event as obsolete.
 *                      Added MPI2_EVENT_SAS_TOPO_LR_UNSUPPORTED_PHY define.
 *  11-10-10  02.00.16  Added MPI2_FW_DOWNLOAD_ITYPE_MIN_PRODUCT_SPECIFIC.
 *  02-23-11  02.00.17  Added SAS NOTIFY Primitive event, and added
 *                      SASNotifyPrimitiveMasks field to
 *                      MPI2_EVENT_NOTIFICATION_REQUEST.
 *                      Added Temperature Threshold Event.
 *                      Added Host Message Event.
 *                      Added Send Host Message request and reply.
 *  05-25-11  02.00.18  For Extended Image Header, added
 *                      MPI2_EXT_IMAGE_TYPE_MIN_PRODUCT_SPECIFIC and
 *                      MPI2_EXT_IMAGE_TYPE_MAX_PRODUCT_SPECIFIC defines.
 *                      Deprecated MPI2_EXT_IMAGE_TYPE_MAX define.
```



```
 *  08-24-11  02.00.19  Added PhysicalPort field to
 *                      MPI2_EVENT_DATA_SAS_DEVICE_STATUS_CHANGE structure.
 *                      Marked MPI2_PM_CONTROL_FEATURE_PCIE_LINK as obsolete.
 *  11-18-11  02.00.20  Incorporating additions for MPI v2.5.
 *  03-29-12  02.00.21  Added a product specific range to event values.
 *  07-26-12  02.00.22  Added MPI2_IOCFACTS_EXCEPT_PARTIAL_MEMORY_FAILURE.
 *                      Added ElapsedSeconds field to
 *                      MPI2_EVENT_DATA_IR_OPERATION_STATUS.
 *  08-19-13  02.00.23  For IOCInit, added MPI2_IOCINIT_MSGFLAG_RDPQ_ARRAY_MODE
 *                      and MPI2_IOC_INIT_RDPQ_ARRAY_ENTRY.
 *                      Added MPI2_IOCFACTS_CAPABILITY_RDPQ_ARRAY_CAPABLE.
 *                      Added MPI2_FW_DOWNLOAD_ITYPE_PUBLIC_KEY.
 *                      Added Encrypted Hash Extended Image.
 *  12-05-13  02.00.24  Added MPI25_HASH_IMAGE_TYPE_BIOS.
 *  --------------------------------------------------------------------------
 */

#ifndef MPI2_IOC_H
#define MPI2_IOC_H

/*****************************************************************************
*
*               IOC Messages
*
*****************************************************************************/

/*****************************************************************************
*  IOCInit message
*****************************************************************************/

/* IOCInit Request message */
typedef struct _MPI2_IOC_INIT_REQUEST
{
    U8                      WhoInit;                        /* 0x00 */
    U8                      Reserved1;                      /* 0x01 */
    U8                      ChainOffset;                    /* 0x02 */
    U8                      Function;                       /* 0x03 */
    U16                     Reserved2;                      /* 0x04 */
    U8                      Reserved3;                      /* 0x06 */
    U8                      MsgFlags;                       /* 0x07 */
    U8                      VP_ID;                          /* 0x08 */
    U8                      VF_ID;                          /* 0x09 */
    U16                     Reserved4;                      /* 0x0A */
    U16                     MsgVersion;                     /* 0x0C */
    U16                     HeaderVersion;                  /* 0x0E */
    U32                     Reserved5;                      /* 0x10 */
    U16                     Reserved6;                      /* 0x14 */
    U8                      Reserved7;                      /* 0x16 */
    U8                      HostMSIxVectors;                /* 0x17 */
    U16                     Reserved8;                      /* 0x18 */
    U32                     Reserved6;                      /* 0x14 */
    U16                     Reserved7;                      /* 0x18 */
    U16                     SystemRequestFrameSize;         /* 0x1A */
    U16                     ReplyDescriptorPostQueueDepth;  /* 0x1C */
    U16                     ReplyFreeQueueDepth;            /* 0x1E */
    U32                     SenseBufferAddressHigh;         /* 0x20 */
    U32                     SystemReplyAddressHigh;         /* 0x24 */
    U64                     SystemRequestFrameBaseAddress;  /* 0x28 */
    U64                     ReplyDescriptorPostQueueAddress;/* 0x30 */
    U64                     ReplyFreeQueueAddress;          /* 0x38 */
    U64                     TimeStamp;                      /* 0x40 */
} MPI2_IOC_INIT_REQUEST, MPI2_POINTER PTR_MPI2_IOC_INIT_REQUEST,
  Mpi2IOCInitRequest_t, MPI2_POINTER pMpi2IOCInitRequest_t;

/* WhoInit values */
#define MPI2_WHOINIT_NOT_INITIALIZED            (0x00)
```

```
#define MPI2_WHOINIT_SYSTEM_BIOS                (0x01)
#define MPI2_WHOINIT_ROM_BIOS                   (0x02)
#define MPI2_WHOINIT_PCI_PEER                   (0x03)
#define MPI2_WHOINIT_HOST_DRIVER                (0x04)
#define MPI2_WHOINIT_MANUFACTURER               (0x05)

/* MsgFlags */
#define MPI2_IOCINIT_MSGFLAG_RDPQ_ARRAY_MODE    (0x01)

/* MsgVersion */
#define MPI2_IOCINIT_MSGVERSION_MAJOR_MASK      (0xFF00)
#define MPI2_IOCINIT_MSGVERSION_MAJOR_SHIFT     (8)
#define MPI2_IOCINIT_MSGVERSION_MINOR_MASK      (0x00FF)
#define MPI2_IOCINIT_MSGVERSION_MINOR_SHIFT     (0)

/* HeaderVersion */
#define MPI2_IOCINIT_HDRVERSION_UNIT_MASK       (0xFF00)
#define MPI2_IOCINIT_HDRVERSION_UNIT_SHIFT      (8)
#define MPI2_IOCINIT_HDRVERSION_DEV_MASK        (0x00FF)
#define MPI2_IOCINIT_HDRVERSION_DEV_SHIFT       (0)

/* minimum depth for a Reply Descriptor Post Queue */
/* minimum depth for the Reply Descriptor Post Queue */
#define MPI2_RDPQ_DEPTH_MIN                     (16)

/* Reply Descriptor Post Queue Array Entry */
typedef struct _MPI2_IOC_INIT_RDPQ_ARRAY_ENTRY
{
    U64                 RDPQBaseAddress;                /* 0x00 */
    U32                 Reserved1;                      /* 0x08 */
    U32                 Reserved2;                      /* 0x0C */
} MPI2_IOC_INIT_RDPQ_ARRAY_ENTRY,
  MPI2_POINTER PTR_MPI2_IOC_INIT_RDPQ_ARRAY_ENTRY,
  Mpi2IOCInitRDPQArrayEntry, MPI2_POINTER pMpi2IOCInitRDPQArrayEntry;

/* IOCInit Reply message */
typedef struct _MPI2_IOC_INIT_REPLY
{
    U8                  WhoInit;                        /* 0x00 */
    U8                  Reserved1;                      /* 0x01 */
    U8                  MsgLength;                      /* 0x02 */
    U8                  Function;                       /* 0x03 */
    U16                 Reserved2;                      /* 0x04 */
    U8                  Reserved3;                      /* 0x06 */
    U8                  MsgFlags;                       /* 0x07 */
    U8                  VP_ID;                          /* 0x08 */
    U8                  VF_ID;                          /* 0x09 */
    U16                 Reserved4;                      /* 0x0A */
    U16                 Reserved5;                      /* 0x0C */
    U16                 IOCStatus;                      /* 0x0E */
    U32                 IOCLogInfo;                     /* 0x10 */
} MPI2_IOC_INIT_REPLY, MPI2_POINTER PTR_MPI2_IOC_INIT_REPLY,
  unchanged_portion_omitted_
  Mpi2IOCFactsRequest_t, MPI2_POINTER pMpi2IOCFactsRequest_t;


/* IOCFacts Reply message */
typedef struct _MPI2_IOC_FACTS_REPLY
{
    U16                 MsgVersion;                     /* 0x00 */
    U8                  MsgLength;                      /* 0x02 */
    U8                  Function;                       /* 0x03 */
    U16                 HeaderVersion;                  /* 0x04 */
    U8                  IOCNumber;                      /* 0x06 */
    U8                  MsgFlags;                       /* 0x07 */
    U8                  VP_ID;                          /* 0x08 */
```



```
    U8                  VF_ID;                          /* 0x09 */
    U16                 Reserved1;                      /* 0x0A */
    U16                 IOCExceptions;                  /* 0x0C */
    U16                 IOCStatus;                      /* 0x0E */
    U32                 IOCLogInfo;                     /* 0x10 */
    U8                  MaxChainDepth;                  /* 0x14 */
    U8                  WhoInit;                        /* 0x15 */
    U8                  NumberOfPorts;                  /* 0x16 */
    U8                  MaxMSIxVectors;                 /* 0x17 */
    U8                  Reserved2;                      /* 0x17 */
    U16                 RequestCredit;                  /* 0x18 */
    U16                 ProductID;                      /* 0x1A */
    U32                 IOCCapabilities;                /* 0x1C */
    MPI2_VERSION_UNION  FWVersion;                      /* 0x20 */
    U16                 IOCRequestFrameSize;            /* 0x24 */
    U16                 IOCMaxChainSegmentSize;         /* 0x26 */ /* MPI 2.
    U16                 Reserved3;                      /* 0x26 */
    U16                 MaxInitiators;                  /* 0x28 */
    U16                 MaxTargets;                     /* 0x2A */
    U16                 MaxSasExpanders;                /* 0x2C */
    U16                 MaxEnclosures;                  /* 0x2E */
    U16                 ProtocolFlags;                  /* 0x30 */
    U16                 HighPriorityCredit;             /* 0x32 */
    U16                 MaxReplyDescriptorPostQueueDepth; /* 0x34 */
    U8                  ReplyFrameSize;                 /* 0x36 */
    U8                  MaxVolumes;                     /* 0x37 */
    U16                 MaxDevHandle;                   /* 0x38 */
    U16                 MaxPersistentEntries;           /* 0x3A */
    U16                 MinDevHandle;                   /* 0x3C */
    U16                 Reserved4;                      /* 0x3E */
    U32                 Reserved4;                      /* 0x3C */
} MPI2_IOC_FACTS_REPLY, MPI2_POINTER PTR_MPI2_IOC_FACTS_REPLY,
  Mpi2IOCFactsReply_t, MPI2_POINTER pMpi2IOCFactsReply_t;

/* MsgVersion */
#define MPI2_IOCFACTS_MSGVERSION_MAJOR_MASK             (0xFF00)
#define MPI2_IOCFACTS_MSGVERSION_MAJOR_SHIFT            (8)
#define MPI2_IOCFACTS_MSGVERSION_MINOR_MASK             (0x00FF)
#define MPI2_IOCFACTS_MSGVERSION_MINOR_SHIFT            (0)

/* HeaderVersion */
#define MPI2_IOCFACTS_HDRVERSION_UNIT_MASK              (0xFF00)
#define MPI2_IOCFACTS_HDRVERSION_UNIT_SHIFT             (8)
#define MPI2_IOCFACTS_HDRVERSION_DEV_MASK               (0x00FF)
#define MPI2_IOCFACTS_HDRVERSION_DEV_SHIFT              (0)

/* IOCExceptions */
#define MPI2_IOCFACTS_EXCEPT_PARTIAL_MEMORY_FAILURE     (0x0200)
#define MPI2_IOCFACTS_EXCEPT_IR_FOREIGN_CONFIG_MAX      (0x0100)

#define MPI2_IOCFACTS_EXCEPT_BOOTSTAT_MASK              (0x00E0)
#define MPI2_IOCFACTS_EXCEPT_BOOTSTAT_GOOD              (0x0000)
#define MPI2_IOCFACTS_EXCEPT_BOOTSTAT_BACKUP            (0x0020)
#define MPI2_IOCFACTS_EXCEPT_BOOTSTAT_RESTORED          (0x0040)
#define MPI2_IOCFACTS_EXCEPT_BOOTSTAT_CORRUPT_BACKUP    (0x0060)

#define MPI2_IOCFACTS_EXCEPT_METADATA_UNSUPPORTED       (0x0010)
#define MPI2_IOCFACTS_EXCEPT_MANUFACT_CHECKSUM_FAIL     (0x0008)
#define MPI2_IOCFACTS_EXCEPT_FW_CHECKSUM_FAIL           (0x0004)
#define MPI2_IOCFACTS_EXCEPT_RAID_CONFIG_INVALID        (0x0002)
#define MPI2_IOCFACTS_EXCEPT_CONFIG_CHECKSUM_FAIL       (0x0001)

/* defines for WhoInit field are after the IOCInit Request */

/* ProductID field uses MPI2_FW_HEADER_PID_ */
```

```
 362 /* IOCCapabilities */
 363 #define MPI2_IOCFACTS_CAPABILITY_RDPQ_ARRAY_CAPABLE     (0x00040000)
 364 #define MPI25_IOCFACTS_CAPABILITY_FAST_PATH_CAPABLE     (0x00020000)
 365 #define MPI2_IOCFACTS_CAPABILITY_HOST_BASED_DISCOVERY   (0x00010000)
 366 #define MPI2_IOCFACTS_CAPABILITY_MSI_X_INDEX            (0x00008000)
 367 #define MPI2_IOCFACTS_CAPABILITY_RAID_ACCELERATOR       (0x00004000)
 368 #define MPI2_IOCFACTS_CAPABILITY_EVENT_REPLAY           (0x00002000)
 369 #define MPI2_IOCFACTS_CAPABILITY_INTEGRATED_RAID        (0x00001000)
 370 #define MPI2_IOCFACTS_CAPABILITY_TLR                    (0x00000800)
 371 #define MPI2_IOCFACTS_CAPABILITY_MULTICAST              (0x00000100)
 372 #define MPI2_IOCFACTS_CAPABILITY_BIDIRECTIONAL_TARGET   (0x00000080)
 373 #define MPI2_IOCFACTS_CAPABILITY_EEDP                   (0x00000040)
 374 #define MPI2_IOCFACTS_CAPABILITY_EXTENDED_BUFFER        (0x00000020)
 375 #define MPI2_IOCFACTS_CAPABILITY_SNAPSHOT_BUFFER        (0x00000010)
 376 #define MPI2_IOCFACTS_CAPABILITY_DIAG_TRACE_BUFFER      (0x00000008)
 377 #define MPI2_IOCFACTS_CAPABILITY_TASK_SET_FULL_HANDLING (0x00000004)

 379 /* ProtocolFlags */
 380 #define MPI2_IOCFACTS_PROTOCOL_SCSI_TARGET              (0x0001)
 381 #define MPI2_IOCFACTS_PROTOCOL_SCSI_INITIATOR           (0x0002)


 384 /****************************************************************************
 385 *  PortFacts message
 386 ****************************************************************************/

 388 /* PortFacts Request message */
 389 typedef struct _MPI2_PORT_FACTS_REQUEST
 390 {
 391     U16                     Reserved1;                  /* 0x00 */
 392     U8                      ChainOffset;                /* 0x02 */
 393     U8                      Function;                   /* 0x03 */
 394     U16                     Reserved2;                  /* 0x04 */
 395     U8                      PortNumber;                 /* 0x06 */
 396     U8                      MsgFlags;                   /* 0x07 */
 397     U8                      VP_ID;                      /* 0x08 */
 398     U8                      VF_ID;                      /* 0x09 */
 399     U16                     Reserved3;                  /* 0x0A */
 400 } MPI2_PORT_FACTS_REQUEST, MPI2_POINTER PTR_MPI2_PORT_FACTS_REQUEST,
_____unchanged_portion_omitted_
 472   Mpi2PortEnableReply_t, MPI2_POINTER pMpi2PortEnableReply_t;


 475 /****************************************************************************
 476 *  EventNotification message
 477 ****************************************************************************/

 479 /* EventNotification Request message */
 480 #define MPI2_EVENT_NOTIFY_EVENTMASK_WORDS           (4)

 482 typedef struct _MPI2_EVENT_NOTIFICATION_REQUEST
 483 {
 484     U16                     Reserved1;                  /* 0x00 */
 485     U8                      ChainOffset;                /* 0x02 */
 486     U8                      Function;                   /* 0x03 */
 487     U16                     Reserved2;                  /* 0x04 */
 488     U8                      Reserved3;                  /* 0x06 */
 489     U8                      MsgFlags;                   /* 0x07 */
 490     U8                      VP_ID;                      /* 0x08 */
 491     U8                      VF_ID;                      /* 0x09 */
 492     U16                     Reserved4;                  /* 0x0A */
 493     U32                     Reserved5;                  /* 0x0C */
 494     U32                     Reserved6;                  /* 0x10 */
 495     U32                     EventMasks[MPI2_EVENT_NOTIFY_EVENTMASK_WORDS];/* 0x1
 496     U16                     SASBroadcastPrimitiveMasks; /* 0x24 */
 497     U16                     SASNotifyPrimitiveMasks;    /* 0x26 */
```



```
 448     U16                     Reserved7;                  /* 0x26 */
 498     U32                     Reserved8;                  /* 0x28 */
 499 } MPI2_EVENT_NOTIFICATION_REQUEST,
_____unchanged_portion_omitted_
 524   Mpi2EventNotificationReply_t, MPI2_POINTER pMpi2EventNotificationReply_t;

 526 /* AckRequired */
 527 #define MPI2_EVENT_NOTIFICATION_ACK_NOT_REQUIRED    (0x00)
 528 #define MPI2_EVENT_NOTIFICATION_ACK_REQUIRED        (0x01)

 530 /* Event */
 531 #define MPI2_EVENT_LOG_DATA                         (0x0001)
 532 #define MPI2_EVENT_STATE_CHANGE                     (0x0002)
 533 #define MPI2_EVENT_HARD_RESET_RECEIVED              (0x0005)
 534 #define MPI2_EVENT_EVENT_CHANGE                     (0x000A)
 535 #define MPI2_EVENT_TASK_SET_FULL                    (0x000E) /* obsolete */
 486 #define MPI2_EVENT_TASK_SET_FULL                    (0x000E)
 536 #define MPI2_EVENT_SAS_DEVICE_STATUS_CHANGE         (0x000F)
 537 #define MPI2_EVENT_IR_OPERATION_STATUS              (0x0014)
 538 #define MPI2_EVENT_SAS_DISCOVERY                    (0x0016)
 539 #define MPI2_EVENT_SAS_BROADCAST_PRIMITIVE          (0x0017)
 540 #define MPI2_EVENT_SAS_INIT_DEVICE_STATUS_CHANGE    (0x0018)
 541 #define MPI2_EVENT_SAS_INIT_TABLE_OVERFLOW          (0x0019)
 542 #define MPI2_EVENT_SAS_TOPOLOGY_CHANGE_LIST         (0x001C)
 543 #define MPI2_EVENT_SAS_ENCL_DEVICE_STATUS_CHANGE    (0x001D)
 544 #define MPI2_EVENT_IR_VOLUME                        (0x001E)
 545 #define MPI2_EVENT_IR_PHYSICAL_DISK                 (0x001F)
 546 #define MPI2_EVENT_IR_CONFIGURATION_CHANGE_LIST     (0x0020)
 547 #define MPI2_EVENT_LOG_ENTRY_ADDED                  (0x0021)
 548 #define MPI2_EVENT_SAS_PHY_COUNTER                  (0x0022)
 549 #define MPI2_EVENT_GPIO_INTERRUPT                   (0x0023)
 550 #define MPI2_EVENT_HOST_BASED_DISCOVERY_PHY         (0x0024)
 551 #define MPI2_EVENT_SAS_QUIESCE                      (0x0025)
 552 #define MPI2_EVENT_SAS_NOTIFY_PRIMITIVE             (0x0026)
 553 #define MPI2_EVENT_TEMP_THRESHOLD                   (0x0027)
 554 #define MPI2_EVENT_HOST_MESSAGE                     (0x0028)
 555 #define MPI2_EVENT_POWER_PERFORMANCE_CHANGE         (0x0029)
 556 #define MPI2_EVENT_MIN_PRODUCT_SPECIFIC             (0x006E)
 557 #define MPI2_EVENT_MAX_PRODUCT_SPECIFIC             (0x007F)


 560 /* Log Entry Added Event data */

 562 /* the following structure matches MPI2_LOG_0_ENTRY in mpi2_cnfg.h */
 563 #define MPI2_EVENT_DATA_LOG_DATA_LENGTH             (0x1C)

 565 typedef struct _MPI2_EVENT_DATA_LOG_ENTRY_ADDED
 566 {
 567     U64         TimeStamp;                          /* 0x00 */
 568     U32         Reserved1;                          /* 0x08 */
 569     U16         LogSequence;                        /* 0x0C */
 570     U16         LogEntryQualifier;                  /* 0x0E */
 571     U8          VP_ID;                              /* 0x10 */
 572     U8          VF_ID;                              /* 0x11 */
 573     U16         Reserved2;                          /* 0x12 */
 574     U8          LogData[MPI2_EVENT_DATA_LOG_DATA_LENGTH];/* 0x14 */
 575 } MPI2_EVENT_DATA_LOG_ENTRY_ADDED,
 576   MPI2_POINTER PTR_MPI2_EVENT_DATA_LOG_ENTRY_ADDED,
 577   Mpi2EventDataLogEntryAdded_t, MPI2_POINTER pMpi2EventDataLogEntryAdded_t;


 580 /* GPIO Interrupt Event data */

 582 typedef struct _MPI2_EVENT_DATA_GPIO_INTERRUPT
 583 {
 584     U8          GPIONum;                            /* 0x00 */
```

```
    U8          Reserved1;                      /* 0x01 */
    U16         Reserved2;                      /* 0x02 */
} MPI2_EVENT_DATA_GPIO_INTERRUPT,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_GPIO_INTERRUPT,
  Mpi2EventDataGpioInterrupt_t, MPI2_POINTER pMpi2EventDataGpioInterrupt_t;


/* Temperature Threshold Event data */

typedef struct _MPI2_EVENT_DATA_TEMPERATURE
{
    U16         Status;                         /* 0x00 */
    U8          SensorNum;                      /* 0x02 */
    U8          Reserved1;                      /* 0x03 */
    U16         CurrentTemperature;             /* 0x04 */
    U16         Reserved2;                      /* 0x06 */
    U32         Reserved3;                      /* 0x08 */
    U32         Reserved4;                      /* 0x0C */
} MPI2_EVENT_DATA_TEMPERATURE,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_TEMPERATURE,
  Mpi2EventDataTemperature_t, MPI2_POINTER pMpi2EventDataTemperature_t;

/* Temperature Threshold Event data Status bits */
#define MPI2_EVENT_TEMPERATURE3_EXCEEDED            (0x0008)
#define MPI2_EVENT_TEMPERATURE2_EXCEEDED            (0x0004)
#define MPI2_EVENT_TEMPERATURE1_EXCEEDED            (0x0002)
#define MPI2_EVENT_TEMPERATURE0_EXCEEDED            (0x0001)


/* Host Message Event data */

typedef struct _MPI2_EVENT_DATA_HOST_MESSAGE
{
    U8          SourceVF_ID;                    /* 0x00 */
    U8          Reserved1;                      /* 0x01 */
    U16         Reserved2;                      /* 0x02 */
    U32         Reserved3;                      /* 0x04 */
    U32         HostData[1];                    /* 0x08 */
} MPI2_EVENT_DATA_HOST_MESSAGE, MPI2_POINTER PTR_MPI2_EVENT_DATA_HOST_MESSAGE,
  Mpi2EventDataHostMessage_t, MPI2_POINTER pMpi2EventDataHostMessage_t;


/* Power Performance Change Event */

typedef struct _MPI2_EVENT_DATA_POWER_PERF_CHANGE
{
    U8          CurrentPowerMode;               /* 0x00 */
    U8          PreviousPowerMode;              /* 0x01 */
    U16         Reserved1;                      /* 0x02 */
} MPI2_EVENT_DATA_POWER_PERF_CHANGE,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_POWER_PERF_CHANGE,
  Mpi2EventDataPowerPerfChange_t, MPI2_POINTER pMpi2EventDataPowerPerfChange_t;

/* defines for CurrentPowerMode and PreviousPowerMode fields */
#define MPI2_EVENT_PM_INIT_MASK             (0xC0)
#define MPI2_EVENT_PM_INIT_UNAVAILABLE      (0x00)
#define MPI2_EVENT_PM_INIT_HOST             (0x40)
#define MPI2_EVENT_PM_INIT_IO_UNIT          (0x80)
#define MPI2_EVENT_PM_INIT_PCIE_DPA         (0xC0)

#define MPI2_EVENT_PM_MODE_MASK             (0x07)
#define MPI2_EVENT_PM_MODE_UNAVAILABLE      (0x00)
#define MPI2_EVENT_PM_MODE_UNKNOWN          (0x01)
#define MPI2_EVENT_PM_MODE_FULL_POWER       (0x04)
#define MPI2_EVENT_PM_MODE_REDUCED_POWER    (0x05)
#define MPI2_EVENT_PM_MODE_STANDBY          (0x06)
```



```


/* Hard Reset Received Event data */

typedef struct _MPI2_EVENT_DATA_HARD_RESET_RECEIVED
{
    U8                      Reserved1;          /* 0x00 */
    U8                      Port;               /* 0x01 */
    U16                     Reserved2;          /* 0x02 */
} MPI2_EVENT_DATA_HARD_RESET_RECEIVED,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_HARD_RESET_RECEIVED,
  Mpi2EventDataHardResetReceived_t,
  MPI2_POINTER pMpi2EventDataHardResetReceived_t;


/* Task Set Full Event data */
/*   this event is obsolete */

typedef struct _MPI2_EVENT_DATA_TASK_SET_FULL
{
    U16                     DevHandle;          /* 0x00 */
    U16                     CurrentDepth;       /* 0x02 */
} MPI2_EVENT_DATA_TASK_SET_FULL, MPI2_POINTER PTR_MPI2_EVENT_DATA_TASK_SET_FULL,
  Mpi2EventDataTaskSetFull_t, MPI2_POINTER pMpi2EventDataTaskSetFull_t;


/* SAS Device Status Change Event data */

typedef struct _MPI2_EVENT_DATA_SAS_DEVICE_STATUS_CHANGE
{
    U16                     TaskTag;            /* 0x00 */
    U8                      ReasonCode;         /* 0x02 */
    U8                      PhysicalPort;       /* 0x03 */
    U8                      Reserved1;          /* 0x03 */
    U8                      ASC;                /* 0x04 */
    U8                      ASCQ;               /* 0x05 */
    U16                     DevHandle;          /* 0x06 */
    U32                     Reserved2;          /* 0x08 */
    U64                     SASAddress;         /* 0x0C */
    U8                      LUN[8];             /* 0x14 */
} MPI2_EVENT_DATA_SAS_DEVICE_STATUS_CHANGE,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_DEVICE_STATUS_CHANGE,
  Mpi2EventDataSasDeviceStatusChange_t,
  MPI2_POINTER pMpi2EventDataSasDeviceStatusChange_t;

/* SAS Device Status Change Event data ReasonCode values */
#define MPI2_EVENT_SAS_DEV_STAT_RC_SMART_DATA                           (0x05)
#define MPI2_EVENT_SAS_DEV_STAT_RC_UNSUPPORTED                          (0x07)
#define MPI2_EVENT_SAS_DEV_STAT_RC_INTERNAL_DEVICE_RESET                (0x08)
#define MPI2_EVENT_SAS_DEV_STAT_RC_TASK_ABORT_INTERNAL                  (0x09)
#define MPI2_EVENT_SAS_DEV_STAT_RC_ABORT_TASK_SET_INTERNAL              (0x0A)
#define MPI2_EVENT_SAS_DEV_STAT_RC_CLEAR_TASK_SET_INTERNAL              (0x0B)
#define MPI2_EVENT_SAS_DEV_STAT_RC_QUERY_TASK_INTERNAL                  (0x0C)
#define MPI2_EVENT_SAS_DEV_STAT_RC_ASYNC_NOTIFICATION                   (0x0D)
#define MPI2_EVENT_SAS_DEV_STAT_RC_CMP_INTERNAL_DEV_RESET               (0x0E)
#define MPI2_EVENT_SAS_DEV_STAT_RC_CMP_TASK_ABORT_INTERNAL              (0x0F)
#define MPI2_EVENT_SAS_DEV_STAT_RC_SATA_INIT_FAILURE                    (0x10)
#define MPI2_EVENT_SAS_DEV_STAT_RC_EXPANDER_REDUCED_FUNCTIONALITY       (0x11)
#define MPI2_EVENT_SAS_DEV_STAT_RC_CMP_EXPANDER_REDUCED_FUNCTIONALITY   (0x12)


/* Integrated RAID Operation Status Event data */

typedef struct _MPI2_EVENT_DATA_IR_OPERATION_STATUS
{
    U16                     VolDevHandle;           /* 0x00 */
```

```
    U16                     Reserved1;                  /* 0x02 */
    U8                      RAIDOperation;              /* 0x04 */
    U8                      PercentComplete;            /* 0x05 */
    U16                     Reserved2;                  /* 0x06 */
    U32                     ElapsedSeconds;             /* 0x08 */
    U32                     Resereved3;                 /* 0x08 */
} MPI2_EVENT_DATA_IR_OPERATION_STATUS,
      unchanged_portion_omitted
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_BROADCAST_PRIMITIVE,
  Mpi2EventDataSasBroadcastPrimitive_t,
  MPI2_POINTER pMpi2EventDataSasBroadcastPrimitive_t;

/* defines for the Primitive field */
#define MPI2_EVENT_PRIMITIVE_CHANGE                     (0x01)
#define MPI2_EVENT_PRIMITIVE_SES                        (0x02)
#define MPI2_EVENT_PRIMITIVE_EXPANDER                   (0x03)
#define MPI2_EVENT_PRIMITIVE_ASYNCHRONOUS_EVENT         (0x04)
#define MPI2_EVENT_PRIMITIVE_RESERVED3                  (0x05)
#define MPI2_EVENT_PRIMITIVE_RESERVED4                  (0x06)
#define MPI2_EVENT_PRIMITIVE_CHANGE0_RESERVED           (0x07)
#define MPI2_EVENT_PRIMITIVE_CHANGE1_RESERVED           (0x08)


/* SAS Notify Primitive Event data */

typedef struct _MPI2_EVENT_DATA_SAS_NOTIFY_PRIMITIVE
{
    U8                      PhyNum;                 /* 0x00 */
    U8                      Port;                   /* 0x01 */
    U8                      Reserved1;              /* 0x02 */
    U8                      Primitive;              /* 0x03 */
} MPI2_EVENT_DATA_SAS_NOTIFY_PRIMITIVE,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_NOTIFY_PRIMITIVE,
  Mpi2EventDataSasNotifyPrimitive_t,
  MPI2_POINTER pMpi2EventDataSasNotifyPrimitive_t;

/* defines for the Primitive field */
#define MPI2_EVENT_NOTIFY_ENABLE_SPINUP                 (0x01)
#define MPI2_EVENT_NOTIFY_POWER_LOSS_EXPECTED           (0x02)
#define MPI2_EVENT_NOTIFY_RESERVED1                     (0x03)
#define MPI2_EVENT_NOTIFY_RESERVED2                     (0x04)


/* SAS Initiator Device Status Change Event data */

typedef struct _MPI2_EVENT_DATA_SAS_INIT_DEV_STATUS_CHANGE
{
    U8                      ReasonCode;             /* 0x00 */
    U8                      PhysicalPort;           /* 0x01 */
    U16                     DevHandle;              /* 0x02 */
    U64                     SASAddress;             /* 0x04 */
} MPI2_EVENT_DATA_SAS_INIT_DEV_STATUS_CHANGE,
      unchanged_portion_omitted
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_TOPOLOGY_CHANGE_LIST,
  Mpi2EventDataSasTopologyChangeList_t,
  MPI2_POINTER pMpi2EventDataSasTopologyChangeList_t;

/* values for the ExpStatus field */
#define MPI2_EVENT_SAS_TOPO_ES_NO_EXPANDER              (0x00)
#define MPI2_EVENT_SAS_TOPO_ES_ADDED                    (0x01)
#define MPI2_EVENT_SAS_TOPO_ES_NOT_RESPONDING           (0x02)
#define MPI2_EVENT_SAS_TOPO_ES_RESPONDING               (0x03)
#define MPI2_EVENT_SAS_TOPO_ES_DELAY_NOT_RESPONDING     (0x04)

/* defines for the LinkRate field */
#define MPI2_EVENT_SAS_TOPO_LR_CURRENT_MASK             (0xF0)
```



```
#define MPI2_EVENT_SAS_TOPO_LR_CURRENT_SHIFT            (4)
#define MPI2_EVENT_SAS_TOPO_LR_PREV_MASK                (0x0F)
#define MPI2_EVENT_SAS_TOPO_LR_PREV_SHIFT               (0)

#define MPI2_EVENT_SAS_TOPO_LR_UNKNOWN_LINK_RATE        (0x00)
#define MPI2_EVENT_SAS_TOPO_LR_PHY_DISABLED             (0x01)
#define MPI2_EVENT_SAS_TOPO_LR_NEGOTIATION_FAILED       (0x02)
#define MPI2_EVENT_SAS_TOPO_LR_SATA_OOB_COMPLETE        (0x03)
#define MPI2_EVENT_SAS_TOPO_LR_PORT_SELECTOR            (0x04)
#define MPI2_EVENT_SAS_TOPO_LR_SMP_RESET_IN_PROGRESS    (0x05)
#define MPI2_EVENT_SAS_TOPO_LR_UNSUPPORTED_PHY          (0x06)
#define MPI2_EVENT_SAS_TOPO_LR_RATE_1_5                 (0x08)
#define MPI2_EVENT_SAS_TOPO_LR_RATE_3_0                 (0x09)
#define MPI2_EVENT_SAS_TOPO_LR_RATE_6_0                 (0x0A)
#define MPI25_EVENT_SAS_TOPO_LR_RATE_12_0               (0x0B)

/* values for the PhyStatus field */
#define MPI2_EVENT_SAS_TOPO_PHYSTATUS_VACANT            (0x80)
#define MPI2_EVENT_SAS_TOPO_PS_MULTIPLEX_CHANGE         (0x10)
/* values for the PhyStatus ReasonCode sub-field */
#define MPI2_EVENT_SAS_TOPO_RC_MASK                     (0x0F)
#define MPI2_EVENT_SAS_TOPO_RC_TARG_ADDED               (0x01)
#define MPI2_EVENT_SAS_TOPO_RC_TARG_NOT_RESPONDING      (0x02)
#define MPI2_EVENT_SAS_TOPO_RC_PHY_CHANGED              (0x03)
#define MPI2_EVENT_SAS_TOPO_RC_NO_CHANGE                (0x04)
#define MPI2_EVENT_SAS_TOPO_RC_DELAY_NOT_RESPONDING     (0x05)


/* SAS Enclosure Device Status Change Event data */

typedef struct _MPI2_EVENT_DATA_SAS_ENCL_DEV_STATUS_CHANGE
{
    U16                     EnclosureHandle;        /* 0x00 */
    U8                      ReasonCode;             /* 0x02 */
    U8                      PhysicalPort;           /* 0x03 */
    U64                     EnclosureLogicalID;     /* 0x04 */
    U16                     NumSlots;               /* 0x0C */
    U16                     StartSlot;              /* 0x0E */
    U32                     PhyBits;                /* 0x10 */
} MPI2_EVENT_DATA_SAS_ENCL_DEV_STATUS_CHANGE,
      unchanged_portion_omitted
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_PHY_COUNTER,
  Mpi2EventDataSasPhyCounter_t, MPI2_POINTER pMpi2EventDataSasPhyCounter_t;

/* use MPI2_SASPHY3_EVENT_CODE_ values from mpi2_cnfg.h for the PhyEventCode fie

/* use MPI2_SASPHY3_COUNTER_TYPE_ values from mpi2_cnfg.h for the CounterType fi

/* use MPI2_SASPHY3_TIME_UNITS_ values from mpi2_cnfg.h for the TimeUnits field

/* use MPI2_SASPHY3_TFLAGS_ values from mpi2_cnfg.h for the ThresholdFlags field


/* SAS Quiesce Event data */

typedef struct _MPI2_EVENT_DATA_SAS_QUIESCE
{
    U8                      ReasonCode;             /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U16                     Reserved2;              /* 0x02 */
    U32                     Reserved3;              /* 0x04 */
} MPI2_EVENT_DATA_SAS_QUIESCE,
  MPI2_POINTER PTR_MPI2_EVENT_DATA_SAS_QUIESCE,
  Mpi2EventDataSasQuiesce_t, MPI2_POINTER pMpi2EventDataSasQuiesce_t;

/* SAS Quiesce Event data ReasonCode values */
```

```
#define MPI2_EVENT_SAS_QUIESCE_RC_STARTED                   (0x01)
#define MPI2_EVENT_SAS_QUIESCE_RC_COMPLETED                 (0x02)


/* Host Based Discovery Phy Event data */

typedef struct _MPI2_EVENT_HBD_PHY_SAS
{
    U8          Flags;                      /* 0x00 */
    U8          NegotiatedLinkRate;         /* 0x01 */
    U8          PhyNum;                     /* 0x02 */
    U8          PhysicalPort;               /* 0x03 */
    U32         Reserved1;                  /* 0x04 */
    U8          InitialFrame[28];           /* 0x08 */
} MPI2_EVENT_HBD_PHY_SAS, MPI2_POINTER PTR_MPI2_EVENT_HBD_PHY_SAS,
  Mpi2EventHbdPhySas_t, MPI2_POINTER pMpi2EventHbdPhySas_t;

/* values for the Flags field */
#define MPI2_EVENT_HBD_SAS_FLAGS_FRAME_VALID        (0x02)
#define MPI2_EVENT_HBD_SAS_FLAGS_SATA_FRAME         (0x01)

/* use MPI2_SAS_NEG_LINK_RATE_ defines from mpi2_cnfg.h for the NegotiatedLinkRa

typedef union _MPI2_EVENT_HBD_DESCRIPTOR
{
    MPI2_EVENT_HBD_PHY_SAS      Sas;
} MPI2_EVENT_HBD_DESCRIPTOR, MPI2_POINTER PTR_MPI2_EVENT_HBD_DESCRIPTOR,
  Mpi2EventHbdDescriptor_t, MPI2_POINTER pMpi2EventHbdDescriptor_t;

typedef struct _MPI2_EVENT_DATA_HBD_PHY
{
    U8                          DescriptorType;     /* 0x00 */
    U8                          Reserved1;          /* 0x01 */
    U16                         Reserved2;          /* 0x02 */
    U32                         Reserved3;          /* 0x04 */
    MPI2_EVENT_HBD_DESCRIPTOR   Descriptor;         /* 0x08 */
} MPI2_EVENT_DATA_HBD_PHY, MPI2_POINTER PTR_MPI2_EVENT_DATA_HBD_PHY,
  Mpi2EventDataHbdPhy_t, MPI2_POINTER pMpi2EventDataMpi2EventDataHbdPhy_t;

/* values for the DescriptorType field */
#define MPI2_EVENT_HBD_DT_SAS               (0x01)



/*****************************************************************************
*  EventAck message
*****************************************************************************/

/* EventAck Request message */
typedef struct _MPI2_EVENT_ACK_REQUEST
{
    U16                     Reserved1;                  /* 0x00 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U16                     Event;                      /* 0x0C */
    U16                     Reserved5;                  /* 0x0E */
    U32                     EventContext;               /* 0x10 */
} MPI2_EVENT_ACK_REQUEST, MPI2_POINTER PTR_MPI2_EVENT_ACK_REQUEST,
______unchanged_portion_omitted_
  Mpi2EventAckReply_t, MPI2_POINTER pMpi2EventAckReply_t;
```



```
/*****************************************************************************
*  SendHostMessage message
*****************************************************************************/

/* SendHostMessage Request message */
typedef struct _MPI2_SEND_HOST_MESSAGE_REQUEST
{
    U16                     HostDataLength;             /* 0x00 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved1;                  /* 0x04 */
    U8                      Reserved2;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U8                      Reserved4;                  /* 0x0C */
    U8                      DestVF_ID;                  /* 0x0D */
    U16                     Reserved5;                  /* 0x0E */
    U32                     Reserved6;                  /* 0x10 */
    U32                     Reserved7;                  /* 0x14 */
    U32                     Reserved8;                  /* 0x18 */
    U32                     Reserved9;                  /* 0x1C */
    U32                     Reserved10;                 /* 0x20 */
    U32                     HostData[1];                /* 0x24 */
} MPI2_SEND_HOST_MESSAGE_REQUEST,
  MPI2_POINTER PTR_MPI2_SEND_HOST_MESSAGE_REQUEST,
  Mpi2SendHostMessageRequest_t, MPI2_POINTER pMpi2SendHostMessageRequest_t;


/* SendHostMessage Reply message */
typedef struct _MPI2_SEND_HOST_MESSAGE_REPLY
{
    U16                     HostDataLength;             /* 0x00 */
    U8                      MsgLength;                  /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved1;                  /* 0x04 */
    U8                      Reserved2;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U16                     Reserved4;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
} MPI2_SEND_HOST_MESSAGE_REPLY, MPI2_POINTER PTR_MPI2_SEND_HOST_MESSAGE_REPLY,
  Mpi2SendHostMessageReply_t, MPI2_POINTER pMpi2SendHostMessageReply_t;


/*****************************************************************************
*  FWDownload message
*****************************************************************************/

/* MPI v2.0 FWDownload Request message */
/* FWDownload Request message */
typedef struct _MPI2_FW_DOWNLOAD_REQUEST
{
    U8                      ImageType;                  /* 0x00 */
    U8                      Reserved1;                  /* 0x01 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
```

```
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved4;              /* 0x0A */
    U32                     TotalImageSize;         /* 0x0C */
    U32                     Reserved5;              /* 0x10 */
    MPI2_MPI_SGE_UNION      SGL;                    /* 0x14 */
} MPI2_FW_DOWNLOAD_REQUEST, MPI2_POINTER PTR_MPI2_FW_DOWNLOAD_REQUEST,
  Mpi2FWDownloadRequest, MPI2_POINTER pMpi2FWDownloadRequest;

#define MPI2_FW_DOWNLOAD_MSGFLGS_LAST_SEGMENT   (0x01)

#define MPI2_FW_DOWNLOAD_ITYPE_FW                   (0x01)
#define MPI2_FW_DOWNLOAD_ITYPE_BIOS                 (0x02)
#define MPI2_FW_DOWNLOAD_ITYPE_MANUFACTURING        (0x06)
#define MPI2_FW_DOWNLOAD_ITYPE_CONFIG_1             (0x07)
#define MPI2_FW_DOWNLOAD_ITYPE_CONFIG_2             (0x08)
#define MPI2_FW_DOWNLOAD_ITYPE_MEGARAID             (0x09)
#define MPI2_FW_DOWNLOAD_ITYPE_COMPLETE             (0x0A)
#define MPI2_FW_DOWNLOAD_ITYPE_COMMON_BOOT_BLOCK    (0x0B)
#define MPI2_FW_DOWNLOAD_ITYPE_PUBLIC_KEY           (0x0C) /* MPI v2.5 and newer
#define MPI2_FW_DOWNLOAD_ITYPE_MIN_PRODUCT_SPECIFIC (0xF0)

/* MPI v2.0 FWDownload TransactionContext Element */
/* FWDownload TransactionContext Element */
typedef struct _MPI2_FW_DOWNLOAD_TCSGE
{
    U8                      Reserved1;              /* 0x00 */
    U8                      ContextSize;            /* 0x01 */
    U8                      DetailsLength;          /* 0x02 */
    U8                      Flags;                  /* 0x03 */
    U32                     Reserved2;              /* 0x04 */
    U32                     ImageOffset;            /* 0x08 */
    U32                     ImageSize;              /* 0x0C */
} MPI2_FW_DOWNLOAD_TCSGE, MPI2_POINTER PTR_MPI2_FW_DOWNLOAD_TCSGE,
  Mpi2FWDownloadTCSGE_t, MPI2_POINTER pMpi2FWDownloadTCSGE_t;


/* MPI v2.5 FWDownload Request message */
typedef struct _MPI25_FW_DOWNLOAD_REQUEST
{
    U8                      ImageType;              /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U8                      ChainOffset;            /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     Reserved2;              /* 0x04 */
    U8                      Reserved3;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved4;              /* 0x0A */
    U32                     TotalImageSize;         /* 0x0C */
    U32                     Reserved5;              /* 0x10 */
    U32                     Reserved6;              /* 0x14 */
    U32                     ImageOffset;            /* 0x18 */
    U32                     ImageSize;              /* 0x1C */
    MPI25_SGE_IO_UNION      SGL;                    /* 0x20 */
} MPI25_FW_DOWNLOAD_REQUEST, MPI2_POINTER PTR_MPI25_FW_DOWNLOAD_REQUEST,
  Mpi25FWDownloadRequest, MPI2_POINTER pMpi25FWDownloadRequest;


/* FWDownload Reply message */
typedef struct _MPI2_FW_DOWNLOAD_REPLY
{
    U8                      ImageType;              /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U8                      MsgLength;              /* 0x02 */
```



```
    U8                      Function;               /* 0x03 */
    U16                     Reserved2;              /* 0x04 */
    U8                      Reserved3;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved4;              /* 0x0A */
    U16                     Reserved5;              /* 0x0C */
    U16                     IOCStatus;              /* 0x0E */
    U32                     IOCLogInfo;             /* 0x10 */
} MPI2_FW_DOWNLOAD_REPLY, MPI2_POINTER PTR_MPI2_FW_DOWNLOAD_REPLY,
  Mpi2FWDownloadReply_t, MPI2_POINTER pMpi2FWDownloadReply_t;


/*****************************************************************************
*  FWUpload message
*****************************************************************************/

/* MPI v2.0 FWUpload Request message */
/* FWUpload Request message */
typedef struct _MPI2_FW_UPLOAD_REQUEST
{
    U8                      ImageType;              /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U8                      ChainOffset;            /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     Reserved2;              /* 0x04 */
    U8                      Reserved3;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved4;              /* 0x0A */
    U32                     Reserved5;              /* 0x0C */
    U32                     Reserved6;              /* 0x10 */
    MPI2_MPI_SGE_UNION      SGL;                    /* 0x14 */
} MPI2_FW_UPLOAD_REQUEST, MPI2_POINTER PTR_MPI2_FW_UPLOAD_REQUEST,
  Mpi2FWUploadRequest_t, MPI2_POINTER pMpi2FWUploadRequest_t;

#define MPI2_FW_UPLOAD_ITYPE_FW_CURRENT         (0x00)
#define MPI2_FW_UPLOAD_ITYPE_FW_FLASH           (0x01)
#define MPI2_FW_UPLOAD_ITYPE_BIOS_FLASH         (0x02)
#define MPI2_FW_UPLOAD_ITYPE_FW_BACKUP          (0x05)
#define MPI2_FW_UPLOAD_ITYPE_MANUFACTURING      (0x06)
#define MPI2_FW_UPLOAD_ITYPE_CONFIG_1           (0x07)
#define MPI2_FW_UPLOAD_ITYPE_CONFIG_2           (0x08)
#define MPI2_FW_UPLOAD_ITYPE_MEGARAID           (0x09)
#define MPI2_FW_UPLOAD_ITYPE_COMPLETE           (0x0A)
#define MPI2_FW_UPLOAD_ITYPE_COMMON_BOOT_BLOCK  (0x0B)

/* MPI v2.0 FWUpload TransactionContext Element */
typedef struct _MPI2_FW_UPLOAD_TCSGE
{
    U8                      Reserved1;              /* 0x00 */
    U8                      ContextSize;            /* 0x01 */
    U8                      DetailsLength;          /* 0x02 */
    U8                      Flags;                  /* 0x03 */
    U32                     Reserved2;              /* 0x04 */
    U32                     ImageOffset;            /* 0x08 */
    U32                     ImageSize;              /* 0x0C */
} MPI2_FW_UPLOAD_TCSGE, MPI2_POINTER PTR_MPI2_FW_UPLOAD_TCSGE,
  Mpi2FWUploadTCSGE_t, MPI2_POINTER pMpi2FWUploadTCSGE_t;


/* MPI v2.5 FWUpload Request message */
typedef struct _MPI25_FW_UPLOAD_REQUEST
{
```

```
1363     U8                      ImageType;                  /* 0x00 */
1364     U8                      Reserved1;                  /* 0x01 */
1365     U8                      ChainOffset;                /* 0x02 */
1366     U8                      Function;                   /* 0x03 */
1367     U16                     Reserved2;                  /* 0x04 */
1368     U8                      Reserved3;                  /* 0x06 */
1369     U8                      MsgFlags;                   /* 0x07 */
1370     U8                      VP_ID;                      /* 0x08 */
1371     U8                      VF_ID;                      /* 0x09 */
1372     U16                     Reserved4;                  /* 0x0A */
1373     U32                     Reserved5;                  /* 0x0C */
1374     U32                     Reserved6;                  /* 0x10 */
1375     U32                     Reserved7;                  /* 0x14 */
1376     U32                     ImageOffset;                /* 0x18 */
1377     U32                     ImageSize;                  /* 0x1C */
1378     MPI25_SGE_IO_UNION      SGL;                        /* 0x20 */
1379 } MPI25_FW_UPLOAD_REQUEST, MPI2_POINTER PTR_MPI25_FW_UPLOAD_REQUEST,
1380   Mpi25FWUploadRequest_t, MPI2_POINTER pMpi25FWUploadRequest_t;


1383 /* FWUpload Reply message */
1384 typedef struct _MPI2_FW_UPLOAD_REPLY
1385 {
1386     U8                      ImageType;                  /* 0x00 */
1387     U8                      Reserved1;                  /* 0x01 */
1388     U8                      MsgLength;                  /* 0x02 */
1389     U8                      Function;                   /* 0x03 */
1390     U16                     Reserved2;                  /* 0x04 */
1391     U8                      Reserved3;                  /* 0x06 */
1392     U8                      MsgFlags;                   /* 0x07 */
1393     U8                      VP_ID;                      /* 0x08 */
1394     U8                      VF_ID;                      /* 0x09 */
1395     U16                     Reserved4;                  /* 0x0A */
1396     U16                     Reserved5;                  /* 0x0C */
1397     U16                     IOCStatus;                  /* 0x0E */
1398     U32                     IOCLogInfo;                 /* 0x10 */
1399     U32                     ActualImageSize;            /* 0x14 */
1400 } MPI2_FW_UPLOAD_REPLY, MPI2_POINTER PTR_MPI2_FW_UPLOAD_REPLY,
______unchanged_portion_omitted_
1453   Mpi2FWImageHeader_t, MPI2_POINTER pMpi2FWImageHeader_t;

1455 /* Signature field */
1456 #define MPI2_FW_HEADER_SIGNATURE_OFFSET         (0x00)
1457 #define MPI2_FW_HEADER_SIGNATURE_MASK           (0xFF000000)
1458 #define MPI2_FW_HEADER_SIGNATURE                (0xEA000000)

1460 /* Signature0 field */
1461 #define MPI2_FW_HEADER_SIGNATURE0_OFFSET        (0x04)
1462 #define MPI2_FW_HEADER_SIGNATURE0               (0x5AFAA55A)

1464 /* Signature1 field */
1465 #define MPI2_FW_HEADER_SIGNATURE1_OFFSET        (0x08)
1466 #define MPI2_FW_HEADER_SIGNATURE1               (0xA55AFAA5)

1468 /* Signature2 field */
1469 #define MPI2_FW_HEADER_SIGNATURE2_OFFSET        (0x0C)
1470 #define MPI2_FW_HEADER_SIGNATURE2               (0x5AA55AFA)


1473 /* defines for using the ProductID field */
1474 #define MPI2_FW_HEADER_PID_TYPE_MASK            (0xF000)
1475 #define MPI2_FW_HEADER_PID_TYPE_SAS             (0x2000)

1477 #define MPI2_FW_HEADER_PID_PROD_MASK                    (0x0F00)
1478 #define MPI2_FW_HEADER_PID_PROD_A                       (0x0000)
1479 #define MPI2_FW_HEADER_PID_PROD_TARGET_INITIATOR_SCSI   (0x0200)
```



```
1480 #define MPI2_FW_HEADER_PID_PROD_IR_SCSI                 (0x0700)


1483 #define MPI2_FW_HEADER_PID_FAMILY_MASK          (0x00FF)
1484 /* SAS ProductID Family bits */
1485 #define MPI2_FW_HEADER_PID_FAMILY_2108_SAS      (0x0013)
1486 #define MPI2_FW_HEADER_PID_FAMILY_2208_SAS      (0x0014)
1487 #define MPI25_FW_HEADER_PID_FAMILY_3108_SAS     (0x0021)
1178 /* SAS */
1179 #define MPI2_FW_HEADER_PID_FAMILY_2108_SAS      (0x0010)
1180 #define MPI2_FW_HEADER_PID_FAMILY_2208_SAS      (0x0011)

1489 /* use MPI2_IOCFACTS_PROTOCOL_ defines for ProtocolFlags field */

1491 /* use MPI2_IOCFACTS_CAPABILITY_ defines for IOCCapabilities field */


1494 #define MPI2_FW_HEADER_IMAGESIZE_OFFSET         (0x2C)
1495 #define MPI2_FW_HEADER_NEXTIMAGE_OFFSET         (0x30)
1496 #define MPI2_FW_HEADER_VERNMHWAT_OFFSET         (0x64)

1498 #define MPI2_FW_HEADER_WHAT_SIGNATURE           (0x29232840)

1500 #define MPI2_FW_HEADER_SIZE                     (0x100)


1503 /* Extended Image Header */
1504 typedef struct _MPI2_EXT_IMAGE_HEADER

1506 {
1507     U8                      ImageType;                  /* 0x00 */
1508     U8                      Reserved1;                  /* 0x01 */
1509     U16                     Reserved2;                  /* 0x02 */
1510     U32                     Checksum;                   /* 0x04 */
1511     U32                     ImageSize;                  /* 0x08 */
1512     U32                     NextImageHeaderOffset;      /* 0x0C */
1513     U32                     PackageVersion;             /* 0x10 */
1514     U32                     Reserved3;                  /* 0x14 */
1515     U32                     Reserved4;                  /* 0x18 */
1516     U32                     Reserved5;                  /* 0x1C */
1517     U8                      IdentifyString[32];         /* 0x20 */
1518 } MPI2_EXT_IMAGE_HEADER, MPI2_POINTER PTR_MPI2_EXT_IMAGE_HEADER,
1519   Mpi2ExtImageHeader_t, MPI2_POINTER pMpi2ExtImageHeader_t;

1521 /* useful offsets */
1522 #define MPI2_EXT_IMAGE_IMAGETYPE_OFFSET         (0x00)
1523 #define MPI2_EXT_IMAGE_IMAGESIZE_OFFSET         (0x08)
1524 #define MPI2_EXT_IMAGE_NEXTIMAGE_OFFSET         (0x0C)

1526 #define MPI2_EXT_IMAGE_HEADER_SIZE              (0x40)

1528 /* defines for the ImageType field */
1529 #define MPI2_EXT_IMAGE_TYPE_UNSPECIFIED             (0x00)
1530 #define MPI2_EXT_IMAGE_TYPE_FW                      (0x01)
1531 #define MPI2_EXT_IMAGE_TYPE_NVDATA                  (0x03)
1532 #define MPI2_EXT_IMAGE_TYPE_BOOTLOADER              (0x04)
1533 #define MPI2_EXT_IMAGE_TYPE_INITIALIZATION          (0x05)
1534 #define MPI2_EXT_IMAGE_TYPE_FLASH_LAYOUT            (0x06)
1535 #define MPI2_EXT_IMAGE_TYPE_SUPPORTED_DEVICES       (0x07)
1536 #define MPI2_EXT_IMAGE_TYPE_MEGARAID                (0x08)
1537 #define MPI2_EXT_IMAGE_TYPE_ENCRYPTED_HASH          (0x09) /* MPI v2.5 and newer
1538 #define MPI2_EXT_IMAGE_TYPE_MIN_PRODUCT_SPECIFIC    (0x80)
1539 #define MPI2_EXT_IMAGE_TYPE_MAX_PRODUCT_SPECIFIC    (0xFF)

1541 #define MPI2_EXT_IMAGE_TYPE_MAX (MPI2_EXT_IMAGE_TYPE_MAX_PRODUCT_SPECIFIC)  /* d
1231 #define MPI2_EXT_IMAGE_TYPE_MAX                 (MPI2_EXT_IMAGE_TYPE_MEGARAID)
```

```
1545 /* FLASH Layout Extended Image Data */

1547 /*
1548  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
1549  * one and check RegionsPerLayout at runtime.
1550  */
1551 #ifndef MPI2_FLASH_NUMBER_OF_REGIONS
1552 #define MPI2_FLASH_NUMBER_OF_REGIONS        (1)
1553 #endif

1555 /*
1556  * Host code (drivers, BIOS, utilities, etc.) should leave this define set to
1557  * one and check NumberOfLayouts at runtime.
1558  */
1559 #ifndef MPI2_FLASH_NUMBER_OF_LAYOUTS
1560 #define MPI2_FLASH_NUMBER_OF_LAYOUTS        (1)
1561 #endif

1563 typedef struct _MPI2_FLASH_REGION
1564 {
1565     U8                      RegionType;             /* 0x00 */
1566     U8                      Reserved1;              /* 0x01 */
1567     U16                     Reserved2;              /* 0x02 */
1568     U32                     RegionOffset;           /* 0x04 */
1569     U32                     RegionSize;             /* 0x08 */
1570     U32                     Reserved3;              /* 0x0C */
1571 } MPI2_FLASH_REGION, MPI2_POINTER PTR_MPI2_FLASH_REGION,
______unchanged_portion_omitted_
1666   Mpi2InitImageFooter_t, MPI2_POINTER pMpi2InitImageFooter_t;

1668 /* defines for the BootFlags field */
1669 #define MPI2_INIT_IMAGE_BOOTFLAGS_OFFSET        (0x00)

1671 /* defines for the ImageSize field */
1672 #define MPI2_INIT_IMAGE_IMAGESIZE_OFFSET        (0x04)

1674 /* defines for the Signature0 field */
1675 #define MPI2_INIT_IMAGE_SIGNATURE0_OFFSET       (0x08)
1676 #define MPI2_INIT_IMAGE_SIGNATURE0              (0x5AA55AEA)

1678 /* defines for the Signature1 field */
1679 #define MPI2_INIT_IMAGE_SIGNATURE1_OFFSET       (0x0C)
1680 #define MPI2_INIT_IMAGE_SIGNATURE1              (0xA55AEAA5)

1682 /* defines for the Signature2 field */
1683 #define MPI2_INIT_IMAGE_SIGNATURE2_OFFSET       (0x10)
1684 #define MPI2_INIT_IMAGE_SIGNATURE2              (0x5AEAA55A)

1686 /* Signature fields as individual bytes */
1687 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_0        (0xEA)
1688 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_1        (0x5A)
1689 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_2        (0xA5)
1690 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_3        (0x5A)

1692 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_4        (0xA5)
1693 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_5        (0xEA)
1694 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_6        (0x5A)
1695 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_7        (0xA5)

1697 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_8        (0x5A)
1698 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_9        (0xA5)
1699 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_A        (0xEA)
1700 #define MPI2_INIT_IMAGE_SIGNATURE_BYTE_B        (0x5A)
```



```
1702 /* defines for the ResetVector field */
1703 #define MPI2_INIT_IMAGE_RESETVECTOR_OFFSET      (0x14)


1706 /* Encrypted Hash Extended Image Data */

1708 typedef struct _MPI25_ENCRYPTED_HASH_ENTRY
1709 {
1710     U8                  HashImageType;          /* 0x00 */
1711     U8                  HashAlgorithm;          /* 0x01 */
1712     U8                  EncryptionAlgorithm;    /* 0x02 */
1713     U8                  Reserved1;              /* 0x03 */
1714     U32                 Reserved2;              /* 0x04 */
1715     U32                 EncryptedHash[1];       /* 0x08 */ /* variable length */
1716 } MPI25_ENCRYPTED_HASH_ENTRY, MPI2_POINTER PTR_MPI25_ENCRYPTED_HASH_ENTRY,
1717   Mpi25EncryptedHashEntry_t, MPI2_POINTER pMpi25EncryptedHashEntry_t;

1719 /* values for HashImageType */
1720 #define MPI25_HASH_IMAGE_TYPE_UNUSED            (0x00)
1721 #define MPI25_HASH_IMAGE_TYPE_FIRMWARE          (0x01)
1722 #define MPI25_HASH_IMAGE_TYPE_BIOS              (0x02)

1724 /* values for HashAlgorithm */
1725 #define MPI25_HASH_ALGORITHM_UNUSED             (0x00)
1726 #define MPI25_HASH_ALGORITHM_SHA256             (0x01)

1728 /* values for EncryptionAlgorithm */
1729 #define MPI25_ENCRYPTION_ALG_UNUSED             (0x00)
1730 #define MPI25_ENCRYPTION_ALG_RSA256             (0x01)

1732 typedef struct _MPI25_ENCRYPTED_HASH_DATA
1733 {
1734     U8                              ImageVersion;           /* 0x00 */
1735     U8                              NumHash;                /* 0x01 */
1736     U16                             Reserved1;              /* 0x02 */
1737     U32                             Reserved2;              /* 0x04 */
1738     MPI25_ENCRYPTED_HASH_ENTRY      EncryptedHashEntry[1];  /* 0x08 */ /* variab
1739 } MPI25_ENCRYPTED_HASH_DATA, MPI2_POINTER PTR_MPI25_ENCRYPTED_HASH_DATA,
1740   Mpi25EncryptedHashData_t, MPI2_POINTER pMpi25EncryptedHashData_t;

1742 /*****************************************************************************
1743 *  PowerManagementControl message
1744 *****************************************************************************/

1746 /* PowerManagementControl Request message */
1747 typedef struct _MPI2_PWR_MGMT_CONTROL_REQUEST
1748 {
1749     U8                      Feature;                /* 0x00 */
1750     U8                      Reserved1;              /* 0x01 */
1751     U8                      ChainOffset;            /* 0x02 */
1752     U8                      Function;               /* 0x03 */
1753     U16                     Reserved2;              /* 0x04 */
1754     U8                      Reserved3;              /* 0x06 */
1755     U8                      MsgFlags;               /* 0x07 */
1756     U8                      VP_ID;                  /* 0x08 */
1757     U8                      VF_ID;                  /* 0x09 */
1758     U16                     Reserved4;              /* 0x0A */
1759     U8                      Parameter1;             /* 0x0C */
1760     U8                      Parameter2;             /* 0x0D */
1761     U8                      Parameter3;             /* 0x0E */
1762     U8                      Parameter4;             /* 0x0F */
1763     U32                     Reserved5;              /* 0x10 */
1764     U32                     Reserved6;              /* 0x14 */
1765 } MPI2_PWR_MGMT_CONTROL_REQUEST, MPI2_POINTER PTR_MPI2_PWR_MGMT_CONTROL_REQUEST,
1766   Mpi2PwrMgmtControlRequest_t, MPI2_POINTER pMpi2PwrMgmtControlRequest_t;
```

```
/* defines for the Feature field */
#define MPI2_PM_CONTROL_FEATURE_DA_PHY_POWER_COND       (0x01)
#define MPI2_PM_CONTROL_FEATURE_PORT_WIDTH_MODULATION   (0x02)
#define MPI2_PM_CONTROL_FEATURE_PCIE_LINK               (0x03) /* obsolete */
#define MPI2_PM_CONTROL_FEATURE_IOC_SPEED               (0x04)
#define MPI2_PM_CONTROL_FEATURE_GLOBAL_PWR_MGMT_MODE    (0x05) /* reserved in MP
#define MPI2_PM_CONTROL_FEATURE_MIN_PRODUCT_SPECIFIC    (0x80)
#define MPI2_PM_CONTROL_FEATURE_MAX_PRODUCT_SPECIFIC    (0xFF)

/* parameter usage for the MPI2_PM_CONTROL_FEATURE_DA_PHY_POWER_COND Feature */
/* Parameter1 contains a PHY number */
/* Parameter2 indicates power condition action using these defines */
#define MPI2_PM_CONTROL_PARAM2_PARTIAL                  (0x01)
#define MPI2_PM_CONTROL_PARAM2_SLUMBER                  (0x02)
#define MPI2_PM_CONTROL_PARAM2_EXIT_PWR_MGMT            (0x03)
/* Parameter3 and Parameter4 are reserved */

/* parameter usage for the MPI2_PM_CONTROL_FEATURE_PORT_WIDTH_MODULATION Feature
/* Parameter1 contains SAS port width modulation group number */
/* Parameter2 indicates IOC action using these defines */
#define MPI2_PM_CONTROL_PARAM2_REQUEST_OWNERSHIP        (0x01)
#define MPI2_PM_CONTROL_PARAM2_CHANGE_MODULATION        (0x02)
#define MPI2_PM_CONTROL_PARAM2_RELINQUISH_OWNERSHIP     (0x03)
/* Parameter3 indicates desired modulation level using these defines */
#define MPI2_PM_CONTROL_PARAM3_25_PERCENT               (0x00)
#define MPI2_PM_CONTROL_PARAM3_50_PERCENT               (0x01)
#define MPI2_PM_CONTROL_PARAM3_75_PERCENT               (0x02)
#define MPI2_PM_CONTROL_PARAM3_100_PERCENT              (0x03)
/* Parameter4 is reserved */

/* this next set (_PCIE_LINK) is obsolete */
/* parameter usage for the MPI2_PM_CONTROL_FEATURE_PCIE_LINK Feature */
/* Parameter1 indicates desired PCIe link speed using these defines */
#define MPI2_PM_CONTROL_PARAM1_PCIE_2_5_GBPS            (0x00) /* obsolete */
#define MPI2_PM_CONTROL_PARAM1_PCIE_5_0_GBPS            (0x01) /* obsolete */
#define MPI2_PM_CONTROL_PARAM1_PCIE_8_0_GBPS            (0x02) /* obsolete */
/* Parameter2 indicates desired PCIe link width using these defines */
#define MPI2_PM_CONTROL_PARAM2_WIDTH_X1                 (0x01) /* obsolete */
#define MPI2_PM_CONTROL_PARAM2_WIDTH_X2                 (0x02) /* obsolete */
#define MPI2_PM_CONTROL_PARAM2_WIDTH_X4                 (0x04) /* obsolete */
#define MPI2_PM_CONTROL_PARAM2_WIDTH_X8                 (0x08) /* obsolete */
/* Parameter3 and Parameter4 are reserved */

/* parameter usage for the MPI2_PM_CONTROL_FEATURE_IOC_SPEED Feature */
/* Parameter1 indicates desired IOC hardware clock speed using these defines */
#define MPI2_PM_CONTROL_PARAM1_FULL_IOC_SPEED           (0x01)
#define MPI2_PM_CONTROL_PARAM1_HALF_IOC_SPEED           (0x02)
#define MPI2_PM_CONTROL_PARAM1_QUARTER_IOC_SPEED        (0x04)
#define MPI2_PM_CONTROL_PARAM1_EIGHTH_IOC_SPEED         (0x08)
/* Parameter2, Parameter3, and Parameter4 are reserved */

/* parameter usage for the MPI2_PM_CONTROL_FEATURE_GLOBAL_PWR_MGMT_MODE Feature
/* Parameter1 indicates host action regarding global power management mode */
#define MPI2_PM_CONTROL_PARAM1_TAKE_CONTROL             (0x01)
#define MPI2_PM_CONTROL_PARAM1_CHANGE_GLOBAL_MODE       (0x02)
#define MPI2_PM_CONTROL_PARAM1_RELEASE_CONTROL          (0x03)
/* Parameter2 indicates the requested global power management mode */
#define MPI2_PM_CONTROL_PARAM2_FULL_PWR_PERF            (0x01)
#define MPI2_PM_CONTROL_PARAM2_REDUCED_PWR_PERF         (0x08)
#define MPI2_PM_CONTROL_PARAM2_STANDBY                  (0x40)
/* Parameter3 and Parameter4 are reserved */


/* PowerManagementControl Reply message */
typedef struct _MPI2_PWR_MGMT_CONTROL_REPLY
```



```
{
    U8                      Feature;                /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U8                      MsgLength;              /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     Reserved2;              /* 0x04 */
    U8                      Reserved3;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved4;              /* 0x0A */
    U16                     Reserved5;              /* 0x0C */
    U16                     IOCStatus;              /* 0x0E */
    U32                     IOCLogInfo;             /* 0x10 */
} MPI2_PWR_MGMT_CONTROL_REPLY, MPI2_POINTER PTR_MPI2_PWR_MGMT_CONTROL_REPLY,
  Mpi2PwrMgmtControlReply_t, MPI2_POINTER pMpi2PwrMgmtControlReply_t;


#endif
```

```
**********************************************************
    5332 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_ra.h
NEX-1888 upstream
**********************************************************
```

```
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 */

/*
 *  Copyright (c) 2009 LSI Corporation.
 *
 *
 *           Name:  mpi2_ra.h
 *          Title:  MPI RAID Accelerator messages and structures
 *  Creation Date:  April 13, 2009
 *
 *  mpi2_ra.h Version:  02.00.00
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  05-06-09  02.00.00  Initial version.
 *  ------------------------------------------------------------------------
 */

#ifndef MPI2_RA_H
#define MPI2_RA_H

/* generic structure for RAID Accelerator Control Block */
typedef struct _MPI2_RAID_ACCELERATOR_CONTROL_BLOCK
{
    U32                 Reserved[8];                /* 0x00 */
    U32                 RaidAcceleratorCDB[1];      /* 0x20 */
} MPI2_RAID_ACCELERATOR_CONTROL_BLOCK,
  MPI2_POINTER PTR_MPI2_RAID_ACCELERATOR_CONTROL_BLOCK,
  Mpi2RAIDAcceleratorControlBlock_t,
  MPI2_POINTER pMpi2RAIDAcceleratorControlBlock_t;
```



```
/*****************************************************************************
*
*        RAID Accelerator Messages
*
*****************************************************************************/

/* RAID Accelerator Request Message */
typedef struct _MPI2_RAID_ACCELERATOR_REQUEST
{
    U16                 Reserved0;                          /* 0x00 */
    U8                  ChainOffset;                        /* 0x02 */
    U8                  Function;                           /* 0x03 */
    U16                 Reserved1;                          /* 0x04 */
    U8                  Reserved2;                          /* 0x06 */
    U8                  MsgFlags;                           /* 0x07 */
    U8                  VP_ID;                              /* 0x08 */
    U8                  VF_ID;                              /* 0x09 */
    U16                 Reserved3;                          /* 0x0A */
    U64                 RaidAcceleratorControlBlockAddress; /* 0x0C */
    U8                  DmaEngineNumber;                    /* 0x14 */
    U8                  Reserved4;                          /* 0x15 */
    U16                 Reserved5;                          /* 0x16 */
    U32                 Reserved6;                          /* 0x18 */
    U32                 Reserved7;                          /* 0x1C */
    U32                 Reserved8;                          /* 0x20 */
} MPI2_RAID_ACCELERATOR_REQUEST, MPI2_POINTER PTR_MPI2_RAID_ACCELERATOR_REQUEST,
  Mpi2RAIDAcceleratorRequest_t, MPI2_POINTER pMpi2RAIDAcceleratorRequest_t;


/* RAID Accelerator Error Reply Message */
typedef struct _MPI2_RAID_ACCELERATOR_REPLY
{
    U16                 Reserved0;                  /* 0x00 */
    U8                  MsgLength;                  /* 0x02 */
    U8                  Function;                   /* 0x03 */
    U16                 Reserved1;                  /* 0x04 */
    U8                  Reserved2;                  /* 0x06 */
    U8                  MsgFlags;                   /* 0x07 */
    U8                  VP_ID;                      /* 0x08 */
    U8                  VF_ID;                      /* 0x09 */
    U16                 Reserved3;                  /* 0x0A */
    U16                 Reserved4;                  /* 0x0C */
    U16                 IOCStatus;                  /* 0x0E */
    U32                 IOCLogInfo;                 /* 0x10 */
    U32                 ProductSpecificData[3];     /* 0x14 */
} MPI2_RAID_ACCELERATOR_REPLY, MPI2_POINTER PTR_MPI2_RAID_ACCELERATOR_REPLY,
  Mpi2RAIDAcceleratorReply_t, MPI2_POINTER pMpi2RAIDAcceleratorReply_t;


#endif
```

```
**********************************************************
   19273 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_raid.h
NEX-1888 upstream
**********************************************************
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 */

/*
 *          Name:  mpi2_raid.h
 *         Title:  MPI Integrated RAID messages and structures
 *  Creation Date:  April 26, 2007
 *
 *    mpi2_raid.h Version:  02.00.10
 *    mpi2_raid.h Version:  02.00.04
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  08-31-07  02.00.01  Modifications to RAID Action request and reply,
 *                      including the Actions and ActionData.
 *  02-29-08  02.00.02  Added MPI2_RAID_ACTION_ADATA_DISABL_FULL_REBUILD.
 *  05-21-08  02.00.03  Added MPI2_RAID_VOL_CREATION_NUM_PHYSDISKS so that
 *                      the PhysDisk array in MPI2_RAID_VOLUME_CREATION_STRUCT
 *                      can be sized by the build environment.
 *  07-30-09  02.00.04  Added proper define for the Use Default Settings bit of
 *                      VolumeCreationFlags and marked the old one as obsolete.
 *  05-12-10  02.00.05  Added MPI2_RAID_VOL_FLAGS_OP_MDC define.
 *  08-24-10  02.00.06  Added MPI2_RAID_ACTION_COMPATIBILITY_CHECK along with
 *                      related structures and defines.
 *                      Added product-specific range to RAID Action values.
 *  11-18-11  02.00.07  Incorporating additions for MPI v2.5.
 *  02-06-12  02.00.08  Added MPI2_RAID_ACTION_PHYSDISK_HIDDEN.
 *  07-26-12  02.00.09  Added ElapsedSeconds field to MPI2_RAID_VOL_INDICATOR.
 *                      Added MPI2_RAID_VOL_FLAGS_ELAPSED_SECONDS_VALID define.
 *  04-17-13  02.00.10  Added MPI25_RAID_ACTION_ADATA_ALLOW_PI.
 *  --------------------------------------------------------------------------
 */

#ifndef MPI2_RAID_H
#define MPI2_RAID_H

/*****************************************************************************
*
*               Integrated RAID Messages
*
*****************************************************************************/

/*****************************************************************************
*  RAID Action messages
*****************************************************************************/

/* ActionDataWord defines for use with MPI2_RAID_ACTION_CREATE_VOLUME action */
#define MPI25_RAID_ACTION_ADATA_ALLOW_PI            (0x80000000)

/* ActionDataWord defines for use with MPI2_RAID_ACTION_DELETE_VOLUME action */
#define MPI2_RAID_ACTION_ADATA_KEEP_LBA0            (0x00000000)
#define MPI2_RAID_ACTION_ADATA_ZERO_LBA0            (0x00000001)
```

```
 86 /* use MPI2_RAIDVOL0_SETTING_ defines from mpi2_cnfg.h for MPI2_RAID_ACTION_CHAN

 88 /* ActionDataWord defines for use with MPI2_RAID_ACTION_DISABLE_ALL_VOLUMES acti
 89 #define MPI2_RAID_ACTION_ADATA_DISABL_FULL_REBUILD  (0x00000001)

 91 /* ActionDataWord for MPI2_RAID_ACTION_SET_RAID_FUNCTION_RATE Action */
 92 typedef struct _MPI2_RAID_ACTION_RATE_DATA
 93 {
 94     U8              RateToChange;               /* 0x00 */
 95     U8              RateOrMode;                 /* 0x01 */
 96     U16             DataScrubDuration;          /* 0x02 */
 97 } MPI2_RAID_ACTION_RATE_DATA, MPI2_POINTER PTR_MPI2_RAID_ACTION_RATE_DATA,
_____unchanged_portion_omitted_
196   Mpi2RaidActionRequest_t, MPI2_POINTER pMpi2RaidActionRequest_t;

198 /* RAID Action request Action values */

200 #define MPI2_RAID_ACTION_INDICATOR_STRUCT           (0x01)
201 #define MPI2_RAID_ACTION_CREATE_VOLUME              (0x02)
202 #define MPI2_RAID_ACTION_DELETE_VOLUME              (0x03)
203 #define MPI2_RAID_ACTION_DISABLE_ALL_VOLUMES        (0x04)
204 #define MPI2_RAID_ACTION_ENABLE_ALL_VOLUMES         (0x05)
205 #define MPI2_RAID_ACTION_PHYSDISK_OFFLINE           (0x0A)
206 #define MPI2_RAID_ACTION_PHYSDISK_ONLINE            (0x0B)
207 #define MPI2_RAID_ACTION_FAIL_PHYSDISK              (0x0F)
208 #define MPI2_RAID_ACTION_ACTIVATE_VOLUME            (0x11)
209 #define MPI2_RAID_ACTION_DEVICE_FW_UPDATE_MODE      (0x15)
210 #define MPI2_RAID_ACTION_CHANGE_VOL_WRITE_CACHE     (0x17)
211 #define MPI2_RAID_ACTION_SET_VOLUME_NAME            (0x18)
212 #define MPI2_RAID_ACTION_SET_RAID_FUNCTION_RATE     (0x19)
213 #define MPI2_RAID_ACTION_ENABLE_FAILED_VOLUME       (0x1C)
214 #define MPI2_RAID_ACTION_CREATE_HOT_SPARE           (0x1D)
215 #define MPI2_RAID_ACTION_DELETE_HOT_SPARE           (0x1E)
216 #define MPI2_RAID_ACTION_SYSTEM_SHUTDOWN_INITIATED  (0x20)
217 #define MPI2_RAID_ACTION_START_RAID_FUNCTION        (0x21)
218 #define MPI2_RAID_ACTION_STOP_RAID_FUNCTION         (0x22)
219 #define MPI2_RAID_ACTION_COMPATIBILITY_CHECK        (0x23)
220 #define MPI2_RAID_ACTION_PHYSDISK_HIDDEN            (0x24)
221 #define MPI2_RAID_ACTION_MIN_PRODUCT_SPECIFIC       (0x80)
222 #define MPI2_RAID_ACTION_MAX_PRODUCT_SPECIFIC       (0xFF)


225 /* RAID Volume Creation Structure */

227 /*
228  * The following define can be customized for the targeted product.
229  */
230 #ifndef MPI2_RAID_VOL_CREATION_NUM_PHYSDISKS
231 #define MPI2_RAID_VOL_CREATION_NUM_PHYSDISKS        (1)
232 #endif

234 typedef struct _MPI2_RAID_VOLUME_PHYSDISK
235 {
236     U8                      RAIDSetNum;                 /* 0x00 */
237     U8                      PhysDiskMap;                /* 0x01 */
238     U16                     PhysDiskDevHandle;          /* 0x02 */
239 } MPI2_RAID_VOLUME_PHYSDISK, MPI2_POINTER PTR_MPI2_RAID_VOLUME_PHYSDISK,
_____unchanged_portion_omitted_
261   MPI2_POINTER PTR_MPI2_RAID_VOLUME_CREATION_STRUCT,
262   Mpi2RaidVolumeCreationStruct_t, MPI2_POINTER pMpi2RaidVolumeCreationStruct_t;

264 /* use MPI2_RAID_VOL_TYPE_ defines from mpi2_cnfg.h for VolumeType */

266 /* defines for the VolumeCreationFlags field */
267 #define MPI2_RAID_VOL_CREATION_DEFAULT_SETTINGS     (0x80000000)
```



```
268 #define MPI2_RAID_VOL_CREATION_BACKGROUND_INIT      (0x00000004) /* MPI 2.0 only
268 #define MPI2_RAID_VOL_CREATION_BACKGROUND_INIT      (0x00000004)
269 #define MPI2_RAID_VOL_CREATION_LOW_LEVEL_INIT       (0x00000002)
270 #define MPI2_RAID_VOL_CREATION_MIGRATE_DATA         (0x00000001)
271 /* The following is an obsolete define.
272  * It must be shifted left 24 bits in order to set the proper bit.
273  */
274 #define MPI2_RAID_VOL_CREATION_USE_DEFAULT_SETTINGS (0x80)


277 /* RAID Online Capacity Expansion Structure */

279 typedef struct _MPI2_RAID_ONLINE_CAPACITY_EXPANSION
280 {
281     U32                     Flags;                      /* 0x00 */
282     U16                     DevHandle0;                 /* 0x04 */
283     U16                     Reserved1;                  /* 0x06 */
284     U16                     DevHandle1;                 /* 0x08 */
285     U16                     Reserved2;                  /* 0x0A */
286 } MPI2_RAID_ONLINE_CAPACITY_EXPANSION,
287   MPI2_POINTER PTR_MPI2_RAID_ONLINE_CAPACITY_EXPANSION,
288   Mpi2RaidOnlineCapacityExpansion_t,
289   MPI2_POINTER pMpi2RaidOnlineCapacityExpansion_t;


292 /* RAID Compatibility Input Structure */

294 typedef struct _MPI2_RAID_COMPATIBILITY_INPUT_STRUCT
295 {
296     U16                     SourceDevHandle;            /* 0x00 */
297     U16                     CandidateDevHandle;         /* 0x02 */
298     U32                     Flags;                      /* 0x04 */
299     U32                     Reserved1;                  /* 0x08 */
300     U32                     Reserved2;                  /* 0x0C */
301 } MPI2_RAID_COMPATIBILITY_INPUT_STRUCT,
302   MPI2_POINTER PTR_MPI2_RAID_COMPATIBILITY_INPUT_STRUCT,
303   Mpi2RaidCompatibilityInputStruct_t,
304   MPI2_POINTER pMpi2RaidCompatibilityInputStruct_t;

306 /* defines for RAID Compatibility Structure Flags field */
307 #define MPI2_RAID_COMPAT_SOURCE_IS_VOLUME_FLAG      (0x00000002)
308 #define MPI2_RAID_COMPAT_REPORT_SOURCE_INFO_FLAG    (0x00000001)


311 /* RAID Volume Indicator Structure */

313 typedef struct _MPI2_RAID_VOL_INDICATOR
314 {
315     U64                     TotalBlocks;                /* 0x00 */
316     U64                     BlocksRemaining;            /* 0x08 */
317     U32                     Flags;                      /* 0x10 */
318     U32                     ElapsedSeconds;             /* 0x14 */
319 } MPI2_RAID_VOL_INDICATOR, MPI2_POINTER PTR_MPI2_RAID_VOL_INDICATOR,
320   Mpi2RaidVolIndicator_t, MPI2_POINTER pMpi2RaidVolIndicator_t;

322 /* defines for RAID Volume Indicator Flags field */
323 #define MPI2_RAID_VOL_FLAGS_ELAPSED_SECONDS_VALID   (0x80000000)

325 #define MPI2_RAID_VOL_FLAGS_OP_MASK                 (0x0000000F)
326 #define MPI2_RAID_VOL_FLAGS_OP_BACKGROUND_INIT      (0x00000000)
327 #define MPI2_RAID_VOL_FLAGS_OP_ONLINE_CAP_EXPANSION (0x00000001)
328 #define MPI2_RAID_VOL_FLAGS_OP_CONSISTENCY_CHECK    (0x00000002)
329 #define MPI2_RAID_VOL_FLAGS_OP_RESYNC               (0x00000003)
330 #define MPI2_RAID_VOL_FLAGS_OP_MDC                  (0x00000004)
```

```
/* RAID Compatibility Result Structure */

typedef struct _MPI2_RAID_COMPATIBILITY_RESULT_STRUCT
{
    U8                      State;                          /* 0x00 */
    U8                      Reserved1;                      /* 0x01 */
    U16                     Reserved2;                      /* 0x02 */
    U32                     GenericAttributes;              /* 0x04 */
    U32                     OEMSpecificAttributes;          /* 0x08 */
    U32                     Reserved3;                      /* 0x0C */
    U32                     Reserved4;                      /* 0x10 */
} MPI2_RAID_COMPATIBILITY_RESULT_STRUCT,
  MPI2_POINTER PTR_MPI2_RAID_COMPATIBILITY_RESULT_STRUCT,
  Mpi2RaidCompatibilityResultStruct_t,
  MPI2_POINTER pMpi2RaidCompatibilityResultStruct_t;

/* defines for RAID Compatibility Result Structure State field */
#define MPI2_RAID_COMPAT_STATE_COMPATIBLE           (0x00)
#define MPI2_RAID_COMPAT_STATE_NOT_COMPATIBLE       (0x01)

/* defines for RAID Compatibility Result Structure GenericAttributes field */
#define MPI2_RAID_COMPAT_GENATTRIB_4K_SECTOR            (0x00000010)

#define MPI2_RAID_COMPAT_GENATTRIB_MEDIA_MASK           (0x0000000C)
#define MPI2_RAID_COMPAT_GENATTRIB_SOLID_STATE_DRIVE    (0x00000008)
#define MPI2_RAID_COMPAT_GENATTRIB_HARD_DISK_DRIVE      (0x00000004)

#define MPI2_RAID_COMPAT_GENATTRIB_PROTOCOL_MASK        (0x00000003)
#define MPI2_RAID_COMPAT_GENATTRIB_SAS_PROTOCOL         (0x00000002)
#define MPI2_RAID_COMPAT_GENATTRIB_SATA_PROTOCOL        (0x00000001)


/* RAID Action Reply ActionData union */
typedef union _MPI2_RAID_ACTION_REPLY_DATA
{
    U32                                 Word[6];
    U32                     Word[5];
    MPI2_RAID_VOL_INDICATOR             RaidVolumeIndicator;
    U16                                 VolDevHandle;
    U8                                  VolumeState;
    U8                                  PhysDiskNum;
    MPI2_RAID_COMPATIBILITY_RESULT_STRUCT   RaidCompatibilityResult;
} MPI2_RAID_ACTION_REPLY_DATA, MPI2_POINTER PTR_MPI2_RAID_ACTION_REPLY_DATA,
```

*unchanged_portion_omitted_*

```
**********************************************************
   16626 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_sas.h
NEX-1888 upstream
**********************************************************
```

```
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 */

/*
 *          Name:  mpi2_sas.h
 *         Title:  MPI Serial Attached SCSI structures and definitions
 *  Creation Date:  February 9, 2007
 *
 *  mpi2_sas.h Version:  02.00.08
 *  mpi2.h Version:  02.00.02
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  06-26-07  02.00.01  Added Clear All Persistent Operation to SAS IO Unit
 *                      Control Request.
 *  10-02-08  02.00.02  Added Set IOC Parameter Operation to SAS IO Unit Control
 *                      Request.
 *  10-28-09  02.00.03  Changed the type of SGL in MPI2_SATA_PASSTHROUGH_REQUEST
 *                      to MPI2_SGE_IO_UNION since it supports chained SGLs.
 *  05-12-10  02.00.04  Modified some comments.
 *  08-11-10  02.00.05  Added NCQ operations to SAS IO Unit Control.
 *  11-18-11  02.00.06  Incorporating additions for MPI v2.5.
 *  07-10-12  02.00.07  Added MPI2_SATA_PT_SGE_UNION for use in the SATA
 *                      Passthrough Request message.
 *  08-19-13  02.00.08  Made MPI2_SAS_OP_TRANSMIT_PORT_SELECT_SIGNAL obsolete
 *                      for anything newer than MPI v2.0.
 *  ------------------------------------------------------------------------
 */

#ifndef MPI2_SAS_H
#define MPI2_SAS_H

/*
 * Values for SASStatus.
 */
#define MPI2_SASSTATUS_SUCCESS                          (0x00)
#define MPI2_SASSTATUS_UNKNOWN_ERROR                    (0x01)
#define MPI2_SASSTATUS_INVALID_FRAME                    (0x02)
#define MPI2_SASSTATUS_UTC_BAD_DEST                     (0x03)
#define MPI2_SASSTATUS_UTC_BREAK_RECEIVED               (0x04)
#define MPI2_SASSTATUS_UTC_CONNECT_RATE_NOT_SUPPORTED   (0x05)
#define MPI2_SASSTATUS_UTC_PORT_LAYER_REQUEST           (0x06)
#define MPI2_SASSTATUS_UTC_PROTOCOL_NOT_SUPPORTED       (0x07)
#define MPI2_SASSTATUS_UTC_STP_RESOURCES_BUSY           (0x08)
#define MPI2_SASSTATUS_UTC_WRONG_DESTINATION            (0x09)
#define MPI2_SASSTATUS_SHORT_INFORMATION_UNIT           (0x0A)
#define MPI2_SASSTATUS_LONG_INFORMATION_UNIT            (0x0B)
```

```
 85 #define MPI2_SASSTATUS_XFER_RDY_INCORRECT_WRITE_DATA    (0x0C)
 86 #define MPI2_SASSTATUS_XFER_RDY_REQUEST_OFFSET_ERROR    (0x0D)
 87 #define MPI2_SASSTATUS_XFER_RDY_NOT_EXPECTED            (0x0E)
 88 #define MPI2_SASSTATUS_DATA_INCORRECT_DATA_LENGTH       (0x0F)
 89 #define MPI2_SASSTATUS_DATA_TOO_MUCH_READ_DATA          (0x10)
 90 #define MPI2_SASSTATUS_DATA_OFFSET_ERROR                (0x11)
 91 #define MPI2_SASSTATUS_SDSF_NAK_RECEIVED                (0x12)
 92 #define MPI2_SASSTATUS_SDSF_CONNECTION_FAILED           (0x13)
 93 #define MPI2_SASSTATUS_INITIATOR_RESPONSE_TIMEOUT       (0x14)


 96 /*
 97  * Values for the SAS DeviceInfo field used in SAS Device Status Change Event
 98  * data and SAS Configuration pages.
 99  */
100 #define MPI2_SAS_DEVICE_INFO_SEP                (0x00004000)
101 #define MPI2_SAS_DEVICE_INFO_ATAPI_DEVICE       (0x00002000)
102 #define MPI2_SAS_DEVICE_INFO_LSI_DEVICE         (0x00001000)
103 #define MPI2_SAS_DEVICE_INFO_DIRECT_ATTACH      (0x00000800)
104 #define MPI2_SAS_DEVICE_INFO_SSP_TARGET         (0x00000400)
105 #define MPI2_SAS_DEVICE_INFO_STP_TARGET         (0x00000200)
106 #define MPI2_SAS_DEVICE_INFO_SMP_TARGET         (0x00000100)
107 #define MPI2_SAS_DEVICE_INFO_SATA_DEVICE        (0x00000080)
108 #define MPI2_SAS_DEVICE_INFO_SSP_INITIATOR      (0x00000040)
109 #define MPI2_SAS_DEVICE_INFO_STP_INITIATOR      (0x00000020)
110 #define MPI2_SAS_DEVICE_INFO_SMP_INITIATOR      (0x00000010)
111 #define MPI2_SAS_DEVICE_INFO_SATA_HOST          (0x00000008)

113 #define MPI2_SAS_DEVICE_INFO_MASK_DEVICE_TYPE   (0x00000007)
114 #define MPI2_SAS_DEVICE_INFO_NO_DEVICE          (0x00000000)
115 #define MPI2_SAS_DEVICE_INFO_END_DEVICE         (0x00000001)
116 #define MPI2_SAS_DEVICE_INFO_EDGE_EXPANDER      (0x00000002)
117 #define MPI2_SAS_DEVICE_INFO_FANOUT_EXPANDER    (0x00000003)


120 /*****************************************************************************
121 *
122 *        SAS Messages
123 *
124 *****************************************************************************/

126 /*****************************************************************************
127 *  SMP Passthrough messages
128 *****************************************************************************/

130 /* SMP Passthrough Request Message */
131 typedef struct _MPI2_SMP_PASSTHROUGH_REQUEST
132 {
133     U8                      PassthroughFlags;   /* 0x00 */
134     U8                      PhysicalPort;       /* 0x01 */
135     U8                      ChainOffset;        /* 0x02 */
136     U8                      Function;           /* 0x03 */
137     U16                     RequestDataLength;  /* 0x04 */
138     U8                      SGLFlags;           /* 0x06 */ /* MPI v2.0 only. Res
140     U8                      SGLFlags;           /* 0x06 */
139     U8                      MsgFlags;           /* 0x07 */
140     U8                      VP_ID;              /* 0x08 */
141     U8                      VF_ID;              /* 0x09 */
142     U16                     Reserved1;          /* 0x0A */
143     U32                     Reserved2;          /* 0x0C */
144     U64                     SASAddress;         /* 0x10 */
145     U32                     Reserved3;          /* 0x18 */
146     U32                     Reserved4;          /* 0x1C */
147     MPI2_SIMPLE_SGE_UNION   SGL;                /* 0x20 */ /* MPI v2.5: IEEE Sim
149     MPI2_SIMPLE_SGE_UNION   SGL;                /* 0x20 */
148 } MPI2_SMP_PASSTHROUGH_REQUEST, MPI2_POINTER PTR_MPI2_SMP_PASSTHROUGH_REQUEST,
```



```
149   Mpi2SmpPassthroughRequest_t, MPI2_POINTER pMpi2SmpPassthroughRequest_t;

151 /* values for PassthroughFlags field */
152 #define MPI2_SMP_PT_REQ_PT_FLAGS_IMMEDIATE      (0x80)

154 /* MPI v2.0: use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */
156 /* values for SGLFlags field are in the SGL section of mpi2.h */


157 /* SMP Passthrough Reply Message */
158 typedef struct _MPI2_SMP_PASSTHROUGH_REPLY
159 {
160     U8                      PassthroughFlags;   /* 0x00 */
161     U8                      PhysicalPort;       /* 0x01 */
162     U8                      MsgLength;          /* 0x02 */
163     U8                      Function;           /* 0x03 */
164     U16                     ResponseDataLength; /* 0x04 */
165     U8                      SGLFlags;           /* 0x06 */
166     U8                      MsgFlags;           /* 0x07 */
167     U8                      VP_ID;              /* 0x08 */
168     U8                      VF_ID;              /* 0x09 */
169     U16                     Reserved1;          /* 0x0A */
170     U8                      Reserved2;          /* 0x0C */
171     U8                      SASStatus;          /* 0x0D */
172     U16                     IOCStatus;          /* 0x0E */
173     U32                     IOCLogInfo;         /* 0x10 */
174     U32                     Reserved3;          /* 0x14 */
175     U8                      ResponseData[4];    /* 0x18 */
176 } MPI2_SMP_PASSTHROUGH_REPLY, MPI2_POINTER PTR_MPI2_SMP_PASSTHROUGH_REPLY,
177   Mpi2SmpPassthroughReply_t, MPI2_POINTER pMpi2SmpPassthroughReply_t;

179 /* values for PassthroughFlags field */
180 #define MPI2_SMP_PT_REPLY_PT_FLAGS_IMMEDIATE    (0x80)

182 /* values for SASStatus field are at the top of this file */


185 /*****************************************************************************
186 *  SATA Passthrough messages
187 *****************************************************************************/

189 typedef union _MPI2_SATA_PT_SGE_UNION
190 {
191     MPI2_SGE_SIMPLE_UNION       MpiSimple;      /* MPI v2.0 only */
192     MPI2_SGE_CHAIN_UNION        MpiChain;       /* MPI v2.0 only */
193     MPI2_IEEE_SGE_SIMPLE_UNION  IeeeSimple;
194     MPI2_IEEE_SGE_CHAIN_UNION   IeeeChain;      /* MPI v2.0 only */
195     MPI25_IEEE_SGE_CHAIN64      IeeeChain64;    /* MPI v2.5 only */
196 } MPI2_SATA_PT_SGE_UNION, MPI2_POINTER PTR_MPI2_SATA_PT_SGE_UNION,
197   Mpi2SataPTSGEUnion_t, MPI2_POINTER pMpi2SataPTSGEUnion_t;


200 /* SATA Passthrough Request Message */
201 typedef struct _MPI2_SATA_PASSTHROUGH_REQUEST
202 {
203     U16                     DevHandle;          /* 0x00 */
204     U8                      ChainOffset;        /* 0x02 */
205     U8                      Function;           /* 0x03 */
206     U16                     PassthroughFlags;   /* 0x04 */
207     U8                      SGLFlags;           /* 0x06 */ /* MPI v2.0 only. Res
198     U8                      SGLFlags;           /* 0x06 */
208     U8                      MsgFlags;           /* 0x07 */
209     U8                      VP_ID;              /* 0x08 */
210     U8                      VF_ID;              /* 0x09 */
211     U16                     Reserved1;          /* 0x0A */
212     U32                     Reserved2;          /* 0x0C */
```

```
213     U32                     Reserved3;          /* 0x10 */
214     U32                     Reserved4;          /* 0x14 */
215     U32                     DataLength;         /* 0x18 */
216     U8                      CommandFIS[20];     /* 0x1C */
217     MPI2_SATA_PT_SGE_UNION  SGL;                /* 0x30 */ /* MPI v2.5: IEEE 64
208     MPI2_SIMPLE_SGE_UNION   SGL;                /* 0x20 */
218 } MPI2_SATA_PASSTHROUGH_REQUEST, MPI2_POINTER PTR_MPI2_SATA_PASSTHROUGH_REQUEST,
219   Mpi2SataPassthroughRequest_t, MPI2_POINTER pMpi2SataPassthroughRequest_t;

221 /* values for PassthroughFlags field */
222 #define MPI2_SATA_PT_REQ_PT_FLAGS_EXECUTE_DIAG      (0x0100)
223 #define MPI2_SATA_PT_REQ_PT_FLAGS_DMA               (0x0020)
224 #define MPI2_SATA_PT_REQ_PT_FLAGS_PIO               (0x0010)
225 #define MPI2_SATA_PT_REQ_PT_FLAGS_UNSPECIFIED_VU    (0x0004)
226 #define MPI2_SATA_PT_REQ_PT_FLAGS_WRITE             (0x0002)
227 #define MPI2_SATA_PT_REQ_PT_FLAGS_READ              (0x0001)

229 /* MPI v2.0: use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */
220 /* values for SGLFlags field are in the SGL section of mpi2.h */


232 /* SATA Passthrough Reply Message */
233 typedef struct _MPI2_SATA_PASSTHROUGH_REPLY
234 {
235     U16                     DevHandle;          /* 0x00 */
236     U8                      MsgLength;          /* 0x02 */
237     U8                      Function;           /* 0x03 */
238     U16                     PassthroughFlags;   /* 0x04 */
239     U8                      SGLFlags;           /* 0x06 */
240     U8                      MsgFlags;           /* 0x07 */
241     U8                      VP_ID;              /* 0x08 */
242     U8                      VF_ID;              /* 0x09 */
243     U16                     Reserved1;          /* 0x0A */
244     U8                      Reserved2;          /* 0x0C */
245     U8                      SASStatus;          /* 0x0D */
246     U16                     IOCStatus;          /* 0x0E */
247     U32                     IOCLogInfo;         /* 0x10 */
248     U8                      StatusFIS[20];      /* 0x14 */
249     U32                     StatusControlRegisters; /* 0x28 */
250     U32                     TransferCount;      /* 0x2C */
251 } MPI2_SATA_PASSTHROUGH_REPLY, MPI2_POINTER PTR_MPI2_SATA_PASSTHROUGH_REPLY,
______unchanged_portion_omitted_
286   MPI2_POINTER PTR_MPI2_SAS_IOUNIT_CONTROL_REQUEST,
287   Mpi2SasIoUnitControlRequest_t, MPI2_POINTER pMpi2SasIoUnitControlRequest_t;

289 /* values for the Operation field */
290 #define MPI2_SAS_OP_CLEAR_ALL_PERSISTENT        (0x02)
291 #define MPI2_SAS_OP_PHY_LINK_RESET              (0x06)
292 #define MPI2_SAS_OP_PHY_HARD_RESET              (0x07)
293 #define MPI2_SAS_OP_PHY_CLEAR_ERROR_LOG         (0x08)
294 #define MPI2_SAS_OP_SEND_PRIMITIVE              (0x0A)
295 #define MPI2_SAS_OP_FORCE_FULL_DISCOVERY        (0x0B)
296 #define MPI2_SAS_OP_TRANSMIT_PORT_SELECT_SIGNAL (0x0C) /* MPI v2.0 only */
287 #define MPI2_SAS_OP_TRANSMIT_PORT_SELECT_SIGNAL (0x0C)
297 #define MPI2_SAS_OP_REMOVE_DEVICE               (0x0D)
298 #define MPI2_SAS_OP_LOOKUP_MAPPING              (0x0E)
299 #define MPI2_SAS_OP_SET_IOC_PARAMETER           (0x0F)
300 #define MPI25_SAS_OP_ENABLE_FP_DEVICE           (0x10)
301 #define MPI25_SAS_OP_DISABLE_FP_DEVICE          (0x11)
302 #define MPI25_SAS_OP_ENABLE_FP_ALL              (0x12)
303 #define MPI25_SAS_OP_DISABLE_FP_ALL             (0x13)
304 #define MPI2_SAS_OP_DEV_ENABLE_NCQ              (0x14)
305 #define MPI2_SAS_OP_DEV_DISABLE_NCQ             (0x15)
306 #define MPI2_SAS_OP_PRODUCT_SPECIFIC_MIN        (0x80)

308 /* values for the PrimFlags field */
```



```
309 #define MPI2_SAS_PRIMFLAGS_SINGLE               (0x08)
310 #define MPI2_SAS_PRIMFLAGS_TRIPLE               (0x02)
311 #define MPI2_SAS_PRIMFLAGS_REDUNDANT            (0x01)

313 /* values for the LookupMethod field */
314 #define MPI2_SAS_LOOKUP_METHOD_SAS_ADDRESS          (0x01)
315 #define MPI2_SAS_LOOKUP_METHOD_SAS_ENCLOSURE_SLOT   (0x02)
316 #define MPI2_SAS_LOOKUP_METHOD_SAS_DEVICE_NAME      (0x03)


319 /* SAS IO Unit Control Reply Message */
320 typedef struct _MPI2_SAS_IOUNIT_CONTROL_REPLY
321 {
322     U8                      Operation;          /* 0x00 */
323     U8                      Reserved1;          /* 0x01 */
324     U8                      MsgLength;          /* 0x02 */
325     U8                      Function;           /* 0x03 */
326     U16                     DevHandle;          /* 0x04 */
327     U8                      IOCParameter;       /* 0x06 */
328     U8                      MsgFlags;           /* 0x07 */
329     U8                      VP_ID;              /* 0x08 */
330     U8                      VF_ID;              /* 0x09 */
331     U16                     Reserved3;          /* 0x0A */
332     U16                     Reserved4;          /* 0x0C */
333     U16                     IOCStatus;          /* 0x0E */
334     U32                     IOCLogInfo;         /* 0x10 */
335 } MPI2_SAS_IOUNIT_CONTROL_REPLY,
______unchanged_portion_omitted_
```

```
**********************************************************
   31281 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_targ.h
NEX-1888 upstream
**********************************************************
```

```
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 */

/*
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 *
 *
 *          Name:  mpi2_targ.h
 *         Title:  MPI Target mode messages and structures
 *  Creation Date:  September 8, 2006
 *
 *  mpi2_targ.h Version: 02.00.06
 *
 *  NOTE: Names (typedefs, defines, etc.) beginning with an MPI25 or Mpi25
 *        prefix are for use only on MPI v2.5 products, and must not be used
 *        with MPI v2.0 products. Unless otherwise noted, names beginning with
 *        MPI2 or Mpi2 are for use with both MPI v2.0 and MPI v2.5 products.
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  08-31-07  02.00.01  Added Command Buffer Data Location Address Space bits to
 *                      BufferPostFlags field of CommandBufferPostBase Request.
 *  02-29-08  02.00.02  Modified various names to make them 32-character unique.
 *  10-02-08  02.00.03  Removed NextCmdBufferOffset from
 *                      MPI2_TARGET_CMD_BUF_POST_BASE_REQUEST.
 *                      Target Status Send Request only takes a single SGE for
 *                      response data.
 *  02-10-10  02.00.04  Added comment to MPI2_TARGET_SSP_RSP_IU structure.
 *  11-18-11  02.00.05  Incorporating additions for MPI v2.5.
 *  11-27-12  02.00.06  Added InitiatorDevHandle field to MPI2_TARGET_MODE_ABORT
 *                      request message structure.
```



```
 *                      Added AbortType MPI2_TARGET_MODE_ABORT_DEVHANDLE and
 *                      MPI2_TARGET_MODE_ABORT_ALL_COMMANDS.
 *  --------------------------------------------------------------------------
 */

#ifndef MPI2_TARG_H
#define MPI2_TARG_H


/*****************************************************************************
*
*        SCSI Target Messages
*
*****************************************************************************/

/****************************************************************************
*  Target Command Buffer Post Base Request
****************************************************************************/

typedef struct _MPI2_TARGET_CMD_BUF_POST_BASE_REQUEST
{
    U8                      BufferPostFlags;        /* 0x00 */
    U8                      Reserved1;              /* 0x01 */
    U8                      ChainOffset;            /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     TotalCmdBuffers;        /* 0x04 */
    U8                      Reserved;               /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved2;              /* 0x0A */
    U32                     Reserved3;              /* 0x0C */
    U16                     CmdBufferLength;        /* 0x10 */
    U16                     Reserved4;              /* 0x12 */
    U32                     BaseAddressLow;         /* 0x14 */
    U32                     BaseAddressHigh;        /* 0x18 */
} MPI2_TARGET_CMD_BUF_POST_BASE_REQUEST,
  MPI2_POINTER PTR_MPI2_TARGET_CMD_BUF_POST_BASE_REQUEST,
  Mpi2TargetCmdBufferPostBaseRequest_t,
  MPI2_POINTER pMpi2TargetCmdBufferPostBaseRequest_t;

/* values for the BufferPostflags field */
#define MPI2_CMD_BUF_POST_BASE_ADDRESS_SPACE_MASK           (0x0C)
#define MPI2_CMD_BUF_POST_BASE_SYSTEM_ADDRESS_SPACE         (0x00)
#define MPI2_CMD_BUF_POST_BASE_IOCDDR_ADDRESS_SPACE         (0x04)
#define MPI2_CMD_BUF_POST_BASE_IOCPLB_ADDRESS_SPACE         (0x08)
#define MPI2_CMD_BUF_POST_BASE_IOCPLBNTA_ADDRESS_SPACE      (0x0C)

#define MPI2_CMD_BUF_POST_BASE_FLAGS_AUTO_POST_ALL          (0x01)


/****************************************************************************
*  Target Command Buffer Post List Request
****************************************************************************/

typedef struct _MPI2_TARGET_CMD_BUF_POST_LIST_REQUEST
{
    U16                     Reserved;               /* 0x00 */
    U8                      ChainOffset;            /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     CmdBufferCount;         /* 0x04 */
    U8                      Reserved1;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved2;              /* 0x0A */
```

```
    U32                     Reserved3;              /* 0x0C */
    U16                     IoIndex[2];             /* 0x10 */
} MPI2_TARGET_CMD_BUF_POST_LIST_REQUEST,
  MPI2_POINTER PTR_MPI2_TARGET_CMD_BUF_POST_LIST_REQUEST,
  Mpi2TargetCmdBufferPostListRequest_t,
  MPI2_POINTER pMpi2TargetCmdBufferPostListRequest_t;

/*****************************************************************************
*  Target Command Buffer Post Base List Reply
*****************************************************************************/

typedef struct _MPI2_TARGET_BUF_POST_BASE_LIST_REPLY
{
    U8                      Flags;                  /* 0x00 */
    U8                      Reserved;               /* 0x01 */
    U8                      MsgLength;              /* 0x02 */
    U8                      Function;               /* 0x03 */
    U16                     Reserved1;              /* 0x04 */
    U8                      Reserved2;              /* 0x06 */
    U8                      MsgFlags;               /* 0x07 */
    U8                      VP_ID;                  /* 0x08 */
    U8                      VF_ID;                  /* 0x09 */
    U16                     Reserved3;              /* 0x0A */
    U16                     Reserved4;              /* 0x0C */
    U16                     IOCStatus;              /* 0x0E */
    U32                     IOCLogInfo;             /* 0x10 */
    U16                     IoIndex;                /* 0x14 */
    U16                     Reserved5;              /* 0x16 */
    U32                     Reserved6;              /* 0x18 */
} MPI2_TARGET_BUF_POST_BASE_LIST_REPLY,
  MPI2_POINTER PTR_MPI2_TARGET_BUF_POST_BASE_LIST_REPLY,
  Mpi2TargetCmdBufferPostBaseListReply_t,
  MPI2_POINTER pMpi2TargetCmdBufferPostBaseListReply_t;

/* Flags defines */
#define MPI2_CMD_BUF_POST_REPLY_IOINDEX_VALID       (0x01)


/*****************************************************************************
*  Command Buffer Formats (with 16 byte CDB)
*****************************************************************************/

typedef struct _MPI2_TARGET_SSP_CMD_BUFFER
{
    U8      FrameType;                              /* 0x00 */
    U8      Reserved1;                              /* 0x01 */
    U16     InitiatorConnectionTag;                 /* 0x02 */
    U32     HashedSourceSASAddress;                 /* 0x04 */
    U16     Reserved2;                              /* 0x08 */
    U16     Flags;                                  /* 0x0A */
    U32     Reserved3;                              /* 0x0C */
    U16     Tag;                                    /* 0x10 */
    U16     TargetPortTransferTag;                  /* 0x12 */
    U32     DataOffset;                             /* 0x14 */
    /* COMMAND information unit starts here */
    U8      LogicalUnitNumber[8];                   /* 0x18 */
    U8      Reserved4;                              /* 0x20 */
    U8      TaskAttribute; /* lower 3 bits */       /* 0x21 */
    U8      Reserved5;                              /* 0x22 */
    U8      AdditionalCDBLength; /* upper 5 bits */ /* 0x23 */
    U8      CDB[16];                                /* 0x24 */
    /* Additional CDB bytes extend past the CDB field */
} MPI2_TARGET_SSP_CMD_BUFFER, MPI2_POINTER PTR_MPI2_TARGET_SSP_CMD_BUFFER,
  Mpi2TargetSspCmdBuffer, MPI2_POINTER pMp2iTargetSspCmdBuffer;

typedef struct _MPI2_TARGET_SSP_TASK_BUFFER
```



```
{
    U8      FrameType;                              /* 0x00 */
    U8      Reserved1;                              /* 0x01 */
    U16     InitiatorConnectionTag;                 /* 0x02 */
    U32     HashedSourceSASAddress;                 /* 0x04 */
    U16     Reserved2;                              /* 0x08 */
    U16     Flags;                                  /* 0x0A */
    U32     Reserved3;                              /* 0x0C */
    U16     Tag;                                    /* 0x10 */
    U16     TargetPortTransferTag;                  /* 0x12 */
    U32     DataOffset;                             /* 0x14 */
    /* TASK information unit starts here */
    U8      LogicalUnitNumber[8];                   /* 0x18 */
    U16     Reserved4;                              /* 0x20 */
    U8      TaskManagementFunction;                 /* 0x22 */
    U8      Reserved5;                              /* 0x23 */
    U16     ManagedTaskTag;                         /* 0x24 */
    U16     Reserved6;                              /* 0x26 */
    U32     Reserved7;                              /* 0x28 */
    U32     Reserved8;                              /* 0x2C */
    U32     Reserved9;                              /* 0x30 */
} MPI2_TARGET_SSP_TASK_BUFFER, MPI2_POINTER PTR_MPI2_TARGET_SSP_TASK_BUFFER,
  Mpi2TargetSspTaskBuffer, MPI2_POINTER pMpi2TargetSspTaskBuffer;

/* mask and shift for HashedSourceSASAddress field */
#define MPI2_TARGET_HASHED_SAS_ADDRESS_MASK     (0xFFFFFF00)
#define MPI2_TARGET_HASHED_SAS_ADDRESS_SHIFT    (8)


/*****************************************************************************
*   MPI v2.0 Target Assist Request
*****************************************************************************/

typedef struct _MPI2_TARGET_ASSIST_REQUEST
{
    U8                  Reserved1;                  /* 0x00 */
    U8                  TargetAssistFlags;          /* 0x01 */
    U8                  ChainOffset;                /* 0x02 */
    U8                  Function;                   /* 0x03 */
    U16                 QueueTag;                   /* 0x04 */
    U8                  Reserved2;                  /* 0x06 */
    U8                  MsgFlags;                   /* 0x07 */
    U8                  VP_ID;                      /* 0x08 */
    U8                  VF_ID;                      /* 0x09 */
    U16                 Reserved3;                  /* 0x0A */
    U16                 IoIndex;                    /* 0x0C */
    U16                 InitiatorConnectionTag;     /* 0x0E */
    U16                 SGLFlags;                   /* 0x10 */
    U8                  SequenceNumber;             /* 0x12 */
    U8                  Reserved4;                  /* 0x13 */
    U8                  SGLOffset0;                 /* 0x14 */
    U8                  SGLOffset1;                 /* 0x15 */
    U8                  SGLOffset2;                 /* 0x16 */
    U8                  SGLOffset3;                 /* 0x17 */
    U32                 SkipCount;                  /* 0x18 */
    U32                 DataLength;                 /* 0x1C */
    U32                 BidirectionalDataLength;    /* 0x20 */
    U16                 IoFlags;                    /* 0x24 */
    U16                 EEDPFlags;                  /* 0x26 */
    U32                 EEDPBlockSize;              /* 0x28 */
    U32                 SecondaryReferenceTag;      /* 0x2C */
    U16                 SecondaryApplicationTag;    /* 0x30 */
    U16                 ApplicationTagTranslationMask;  /* 0x32 */
    U32                 PrimaryReferenceTag;        /* 0x34 */
    U16                 PrimaryApplicationTag;      /* 0x38 */
    U16                 PrimaryApplicationTagMask;  /* 0x3A */
```

```
    U32                 RelativeOffset;                 /* 0x3C */
    U32                 Reserved5;                      /* 0x40 */
    U32                 Reserved6;                      /* 0x44 */
    U32                 Reserved7;                      /* 0x48 */
    U32                 Reserved8;                      /* 0x4C */
    MPI2_SGE_IO_UNION   SGL[1];                         /* 0x50 */
} MPI2_TARGET_ASSIST_REQUEST, MPI2_POINTER PTR_MPI2_TARGET_ASSIST_REQUEST,
  Mpi2TargetAssistRequest_t, MPI2_POINTER pMpi2TargetAssistRequest_t;

/* Target Assist TargetAssistFlags bits */

#define MPI2_TARGET_ASSIST_FLAGS_REPOST_CMD_BUFFER      (0x80)
#define MPI2_TARGET_ASSIST_FLAGS_TLR                    (0x10)
#define MPI2_TARGET_ASSIST_FLAGS_RETRANSMIT             (0x04)
#define MPI2_TARGET_ASSIST_FLAGS_AUTO_STATUS            (0x02)
#define MPI2_TARGET_ASSIST_FLAGS_DATA_DIRECTION         (0x01)

/* Target Assist SGLFlags bits */

/* base values for Data Location Address Space */
#define MPI2_TARGET_ASSIST_SGLFLAGS_ADDR_MASK           (0x0C)
#define MPI2_TARGET_ASSIST_SGLFLAGS_SYSTEM_ADDR         (0x00)
#define MPI2_TARGET_ASSIST_SGLFLAGS_IOCDDR_ADDR         (0x04)
#define MPI2_TARGET_ASSIST_SGLFLAGS_IOCPLB_ADDR         (0x08)
#define MPI2_TARGET_ASSIST_SGLFLAGS_PLBNTA_ADDR         (0x0C)

/* base values for Type */
#define MPI2_TARGET_ASSIST_SGLFLAGS_TYPE_MASK           (0x03)
#define MPI2_TARGET_ASSIST_SGLFLAGS_MPI_TYPE            (0x00)
#define MPI2_TARGET_ASSIST_SGLFLAGS_32IEEE_TYPE         (0x01)
#define MPI2_TARGET_ASSIST_SGLFLAGS_64IEEE_TYPE         (0x02)

/* shift values for each sub-field */
#define MPI2_TARGET_ASSIST_SGLFLAGS_SGL3_SHIFT          (12)
#define MPI2_TARGET_ASSIST_SGLFLAGS_SGL2_SHIFT          (8)
#define MPI2_TARGET_ASSIST_SGLFLAGS_SGL1_SHIFT          (4)
#define MPI2_TARGET_ASSIST_SGLFLAGS_SGL0_SHIFT          (0)

/* Target Assist IoFlags bits */

#define MPI2_TARGET_ASSIST_IOFLAGS_BIDIRECTIONAL        (0x0800)
#define MPI2_TARGET_ASSIST_IOFLAGS_MULTICAST            (0x0400)
#define MPI2_TARGET_ASSIST_IOFLAGS_RECEIVE_FIRST        (0x0200)

/* Target Assist EEDPFlags bits */

#define MPI2_TA_EEDPFLAGS_INC_PRI_REFTAG            (0x8000)
#define MPI2_TA_EEDPFLAGS_INC_SEC_REFTAG            (0x4000)
#define MPI2_TA_EEDPFLAGS_INC_PRI_APPTAG            (0x2000)
#define MPI2_TA_EEDPFLAGS_INC_SEC_APPTAG            (0x1000)

#define MPI2_TA_EEDPFLAGS_CHECK_REFTAG              (0x0400)
#define MPI2_TA_EEDPFLAGS_CHECK_APPTAG              (0x0200)
#define MPI2_TA_EEDPFLAGS_CHECK_GUARD               (0x0100)

#define MPI2_TA_EEDPFLAGS_PASSTHRU_REFTAG           (0x0008)

#define MPI2_TA_EEDPFLAGS_MASK_OP                   (0x0007)
#define MPI2_TA_EEDPFLAGS_NOOP_OP                   (0x0000)
#define MPI2_TA_EEDPFLAGS_CHECK_OP                  (0x0001)
#define MPI2_TA_EEDPFLAGS_STRIP_OP                  (0x0002)
#define MPI2_TA_EEDPFLAGS_CHECK_REMOVE_OP           (0x0003)
#define MPI2_TA_EEDPFLAGS_INSERT_OP                 (0x0004)
#define MPI2_TA_EEDPFLAGS_REPLACE_OP                (0x0006)
#define MPI2_TA_EEDPFLAGS_CHECK_REGEN_OP            (0x0007)
```



```
/*****************************************************************************
*   MPI v2.5 Target Assist Request
*****************************************************************************/

typedef struct _MPI25_TARGET_ASSIST_REQUEST
{
    U8                  Reserved1;                      /* 0x00 */
    U8                  TargetAssistFlags;              /* 0x01 */
    U8                  ChainOffset;                    /* 0x02 */
    U8                  Function;                       /* 0x03 */
    U16                 QueueTag;                       /* 0x04 */
    U8                  Reserved2;                      /* 0x06 */
    U8                  MsgFlags;                       /* 0x07 */
    U8                  VP_ID;                          /* 0x08 */
    U8                  VF_ID;                          /* 0x09 */
    U16                 Reserved3;                      /* 0x0A */
    U16                 IoIndex;                        /* 0x0C */
    U16                 InitiatorConnectionTag;         /* 0x0E */
    U8                  DMAFlags;                       /* 0x10 */
    U8                  Reserved9;                      /* 0x11 */
    U8                  SequenceNumber;                 /* 0x12 */
    U8                  Reserved4;                      /* 0x13 */
    U8                  SGLOffset0;                     /* 0x14 */
    U8                  SGLOffset1;                     /* 0x15 */
    U8                  SGLOffset2;                     /* 0x16 */
    U8                  SGLOffset3;                     /* 0x17 */
    U32                 SkipCount;                      /* 0x18 */
    U32                 DataLength;                     /* 0x1C */
    U32                 BidirectionalDataLength;        /* 0x20 */
    U16                 IoFlags;                        /* 0x24 */
    U16                 EEDPFlags;                      /* 0x26 */
    U16                 EEDPBlockSize;                  /* 0x28 */
    U16                 Reserved10;                     /* 0x2A */
    U32                 SecondaryReferenceTag;          /* 0x2C */
    U16                 SecondaryApplicationTag;        /* 0x30 */
    U16                 ApplicationTagTranslationMask;  /* 0x32 */
    U32                 PrimaryReferenceTag;            /* 0x34 */
    U16                 PrimaryApplicationTag;          /* 0x38 */
    U16                 PrimaryApplicationTagMask;      /* 0x3A */
    U32                 RelativeOffset;                 /* 0x3C */
    U32                 Reserved5;                      /* 0x40 */
    U32                 Reserved6;                      /* 0x44 */
    U32                 Reserved7;                      /* 0x48 */
    U32                 Reserved8;                      /* 0x4C */
    MPI25_SGE_IO_UNION  SGL;                            /* 0x50 */
} MPI25_TARGET_ASSIST_REQUEST, MPI2_POINTER PTR_MPI25_TARGET_ASSIST_REQUEST,
  Mpi25TargetAssistRequest_t, MPI2_POINTER pMpi25TargetAssistRequest_t;

/* use MPI2_TARGET_ASSIST_FLAGS_ defines for the Flags field */

/* Defines for the DMAFlags field
 *  Each setting affects 4 SGLS, from SGL0 to SGL3.
 *      D = Data
 *      C = Cache DIF
 *      I = Interleaved
 *      H = Host DIF
 */
#define MPI25_TA_DMAFLAGS_OP_MASK                   (0x0F)
#define MPI25_TA_DMAFLAGS_OP_D_D_D_D                (0x00)
#define MPI25_TA_DMAFLAGS_OP_D_D_D_C                (0x01)
#define MPI25_TA_DMAFLAGS_OP_D_D_D_I                (0x02)
#define MPI25_TA_DMAFLAGS_OP_D_D_C_C                (0x03)
#define MPI25_TA_DMAFLAGS_OP_D_D_C_I                (0x04)
#define MPI25_TA_DMAFLAGS_OP_D_D_I_I                (0x05)
#define MPI25_TA_DMAFLAGS_OP_D_C_C_C                (0x06)
```

```
392 #define MPI25_TA_DMAFLAGS_OP_D_C_C_I                (0x07)
393 #define MPI25_TA_DMAFLAGS_OP_D_C_I_I                (0x08)
394 #define MPI25_TA_DMAFLAGS_OP_D_I_I_I                (0x09)
395 #define MPI25_TA_DMAFLAGS_OP_D_H_D_D                (0x0A)
396 #define MPI25_TA_DMAFLAGS_OP_D_H_D_C                (0x0B)
397 #define MPI25_TA_DMAFLAGS_OP_D_H_D_I                (0x0C)
398 #define MPI25_TA_DMAFLAGS_OP_D_H_C_C                (0x0D)
399 #define MPI25_TA_DMAFLAGS_OP_D_H_C_I                (0x0E)
400 #define MPI25_TA_DMAFLAGS_OP_D_H_I_I                (0x0F)

402 /* defines for the IoFlags field */
403 #define MPI25_TARGET_ASSIST_IOFLAGS_BIDIRECTIONAL       (0x0800)
404 #define MPI25_TARGET_ASSIST_IOFLAGS_RECEIVE_FIRST       (0x0200)

406 /* defines for the EEDPFlags field */
407 #define MPI25_TA_EEDPFLAGS_INC_PRI_REFTAG               (0x8000)
408 #define MPI25_TA_EEDPFLAGS_INC_SEC_REFTAG               (0x4000)
409 #define MPI25_TA_EEDPFLAGS_INC_PRI_APPTAG               (0x2000)
410 #define MPI25_TA_EEDPFLAGS_INC_SEC_APPTAG               (0x1000)

412 #define MPI25_TA_EEDPFLAGS_CHECK_REFTAG                 (0x0400)
413 #define MPI25_TA_EEDPFLAGS_CHECK_APPTAG                 (0x0200)
414 #define MPI25_TA_EEDPFLAGS_CHECK_GUARD                  (0x0100)

416 #define MPI25_TA_EEDPFLAGS_ESCAPE_MODE_MASK             (0x00C0)
417 #define MPI25_TA_EEDPFLAGS_COMPATIBLE_MODE              (0x0000)
418 #define MPI25_TA_EEDPFLAGS_DO_NOT_DISABLE_MODE          (0x0040)
419 #define MPI25_TA_EEDPFLAGS_APPTAG_DISABLE_MODE          (0x0080)
420 #define MPI25_TA_EEDPFLAGS_APPTAG_REFTAG_DISABLE_MODE   (0x00C0)

422 #define MPI25_TA_EEDPFLAGS_HOST_GUARD_METHOD_MASK       (0x0030)
423 #define MPI25_TA_EEDPFLAGS_T10_CRC_HOST_GUARD           (0x0000)
424 #define MPI25_TA_EEDPFLAGS_IP_CHKSUM_HOST_GUARD         (0x0010)

426 #define MPI25_TA_EEDPFLAGS_PASSTHRU_REFTAG              (0x0008)

428 #define MPI25_TA_EEDPFLAGS_MASK_OP                      (0x0007)
429 #define MPI25_TA_EEDPFLAGS_NOOP_OP                      (0x0000)
430 #define MPI25_TA_EEDPFLAGS_CHECK_OP                     (0x0001)
431 #define MPI25_TA_EEDPFLAGS_STRIP_OP                     (0x0002)
432 #define MPI25_TA_EEDPFLAGS_CHECK_REMOVE_OP              (0x0003)
433 #define MPI25_TA_EEDPFLAGS_INSERT_OP                    (0x0004)
434 #define MPI25_TA_EEDPFLAGS_REPLACE_OP                   (0x0006)
435 #define MPI25_TA_EEDPFLAGS_CHECK_REGEN_OP               (0x0007)


438 /*****************************************************************************
439 *  Target Status Send Request
440 *****************************************************************************/

442 typedef struct _MPI2_TARGET_STATUS_SEND_REQUEST
443 {
444     U8                      Reserved1;              /* 0x00 */
445     U8                      StatusFlags;            /* 0x01 */
446     U8                      ChainOffset;            /* 0x02 */
447     U8                      Function;               /* 0x03 */
448     U16                     QueueTag;               /* 0x04 */
449     U8                      Reserved2;              /* 0x06 */
450     U8                      MsgFlags;               /* 0x07 */
451     U8                      VP_ID;                  /* 0x08 */
452     U8                      VF_ID;                  /* 0x09 */
453     U16                     Reserved3;              /* 0x0A */
454     U16                     IoIndex;                /* 0x0C */
455     U16                     InitiatorConnectionTag; /* 0x0E */
456     U16                     SGLFlags;               /* 0x10 */ /* MPI v2.0 o
457     U16                     Reserved4;              /* 0x12 */
```



```
458     U8                      SGLOffset0;             /* 0x14 */
459     U8                      Reserved5;              /* 0x15 */
460     U16                     Reserved6;              /* 0x16 */
461     U32                     Reserved7;              /* 0x18 */
462     U32                     Reserved8;              /* 0x1C */
463     MPI2_SIMPLE_SGE_UNION   StatusDataSGE;          /* 0x20 */ /* MPI v2.5:
464 } MPI2_TARGET_STATUS_SEND_REQUEST,
465   MPI2_POINTER PTR_MPI2_TARGET_STATUS_SEND_REQUEST,
466   Mpi2TargetStatusSendRequest_t, MPI2_POINTER pMpi2TargetStatusSendRequest_t;

468 /* Target Status Send StatusFlags bits */

470 #define MPI2_TSS_FLAGS_REPOST_CMD_BUFFER            (0x80)
471 #define MPI2_TSS_FLAGS_RETRANSMIT                   (0x04)
472 #define MPI2_TSS_FLAGS_AUTO_GOOD_STATUS             (0x01)

474 /* Target Status Send SGLFlags bits - MPI v2.0 only */
475 /* Data Location Address Space */
476 #define MPI2_TSS_SGLFLAGS_ADDR_MASK                 (0x0C)
477 #define MPI2_TSS_SGLFLAGS_SYSTEM_ADDR               (0x00)
478 #define MPI2_TSS_SGLFLAGS_IOCDDR_ADDR               (0x04)
479 #define MPI2_TSS_SGLFLAGS_IOCPLB_ADDR               (0x08)
480 #define MPI2_TSS_SGLFLAGS_IOCPLBNTA_ADDR            (0x0C)
481 /* Type */
482 #define MPI2_TSS_SGLFLAGS_TYPE_MASK                 (0x03)
483 #define MPI2_TSS_SGLFLAGS_MPI_TYPE                  (0x00)
484 #define MPI2_TSS_SGLFLAGS_IEEE32_TYPE               (0x01)
485 #define MPI2_TSS_SGLFLAGS_IEEE64_TYPE               (0x02)



489 /*
490  * NOTE: The SSP status IU is big-endian. When used on a little-endian system,
491  * this structure properly orders the bytes.
492  */
493 typedef struct _MPI2_TARGET_SSP_RSP_IU
494 {
495     U32     Reserved0[6]; /* reserved for SSP header */ /* 0x00 */

497     /* start of RESPONSE information unit */
498     U32     Reserved1;                                  /* 0x18 */
499     U32     Reserved2;                                  /* 0x1C */
500     U16     Reserved3;                                  /* 0x20 */
501     U8      DataPres; /* lower 2 bits */                /* 0x22 */
502     U8      Status;                                     /* 0x23 */
503     U32     Reserved4;                                  /* 0x24 */
504     U32     SenseDataLength;                            /* 0x28 */
505     U32     ResponseDataLength;                         /* 0x2C */

507     /* start of Response or Sense Data (size may vary dynamically) */
508     U8      ResponseSenseData[4];                       /* 0x30 */
509 } MPI2_TARGET_SSP_RSP_IU, MPI2_POINTER PTR_MPI2_TARGET_SSP_RSP_IU,
510   Mpi2TargetSspRspIu_t, MPI2_POINTER pMpi2TargetSspRspIu_t;


513 /*****************************************************************************
514 *  Target Standard Reply - used with Target Assist or Target Status Send
515 *****************************************************************************/

517 typedef struct _MPI2_TARGET_STANDARD_REPLY
518 {
519     U16                     Reserved;               /* 0x00 */
520     U8                      MsgLength;              /* 0x02 */
521     U8                      Function;               /* 0x03 */
522     U16                     Reserved1;              /* 0x04 */
523     U8                      Reserved2;              /* 0x06 */
```

```
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U16                     Reserved4;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
    U16                     IoIndex;                    /* 0x14 */
    U16                     Reserved5;                  /* 0x16 */
    U32                     TransferCount;              /* 0x18 */
    U32                     BidirectionalTransferCount; /* 0x1C */
} MPI2_TARGET_STANDARD_REPLY, MPI2_POINTER PTR_MPI2_TARGET_STANDARD_REPLY,
  Mpi2TargetErrorReply_t, MPI2_POINTER pMpi2TargetErrorReply_t;


/*****************************************************************************
*  Target Mode Abort Request
*****************************************************************************/

typedef struct _MPI2_TARGET_MODE_ABORT_REQUEST
{
    U8                      AbortType;                  /* 0x00 */
    U8                      Reserved1;                  /* 0x01 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U16                     IoIndexToAbort;             /* 0x0C */
    U16                     InitiatorDevHandle;         /* 0x0E */
    U32                     MidToAbort;                 /* 0x10 */
} MPI2_TARGET_MODE_ABORT, MPI2_POINTER PTR_MPI2_TARGET_MODE_ABORT,
  Mpi2TargetModeAbort_t, MPI2_POINTER pMpi2TargetModeAbort_t;

/* Target Mode Abort AbortType values */

#define MPI2_TARGET_MODE_ABORT_ALL_CMD_BUFFERS      (0x00)
#define MPI2_TARGET_MODE_ABORT_ALL_IO               (0x01)
#define MPI2_TARGET_MODE_ABORT_EXACT_IO             (0x02)
#define MPI2_TARGET_MODE_ABORT_EXACT_IO_REQUEST     (0x03)
#define MPI2_TARGET_MODE_ABORT_IO_REQUEST_AND_IO    (0x04)
#define MPI2_TARGET_MODE_ABORT_DEVHANDLE            (0x05)
#define MPI2_TARGET_MODE_ABORT_ALL_COMMANDS         (0x06)


/*****************************************************************************
*  Target Mode Abort Reply
*****************************************************************************/

typedef struct _MPI2_TARGET_MODE_ABORT_REPLY
{
    U16                     Reserved;                   /* 0x00 */
    U8                      MsgLength;                  /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved1;                  /* 0x04 */
    U8                      Reserved2;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved3;                  /* 0x0A */
    U16                     Reserved4;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
```



```
    U32                     AbortCount;                 /* 0x14 */
} MPI2_TARGET_MODE_ABORT_REPLY, MPI2_POINTER PTR_MPI2_TARGET_MODE_ABORT_REPLY,
  Mpi2TargetModeAbortReply_t, MPI2_POINTER pMpi2TargetModeAbortReply_t;


#endif
```

```
**********************************************************
   27717 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_tool.h
NEX-1888 upstream
**********************************************************
```

```
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 */

/*
 *          Name:  mpi2_tool.h
 *         Title:  MPI diagnostic tool structures and definitions
 *  Creation Date:  March 26, 2007
 *
 *    mpi2_tool.h Version:  02.00.11
 *    mpi2_tool.h Version:  02.00.04
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  12-18-07  02.00.01  Added Diagnostic Buffer Post and Diagnostic Release
 *                      structures and defines.
 *  02-29-08  02.00.02  Modified various names to make them 32-character unique.
 *  05-06-09  02.00.03  Added ISTWI Read Write Tool and Diagnostic CLI Tool.
 *  07-30-09  02.00.04  Added ExtendedType field to DiagnosticBufferPost request
 *                      and reply messages.
 *                      Added MPI2_DIAG_BUF_TYPE_EXTENDED.
 *                      Incremented MPI2_DIAG_BUF_TYPE_COUNT.
 *  05-12-10  02.00.05  Added Diagnostic Data Upload tool.
 *  08-11-10  02.00.06  Added defines that were missing for Diagnostic Buffer
 *                      Post Request.
 *  05-25-11  02.00.07  Added Flags field and related defines to
 *                      MPI2_TOOLBOX_ISTWI_READ_WRITE_REQUEST.
 *  11-18-11  02.00.08  Incorporating additions for MPI v2.5.
 *  07-10-12  02.00.09  Add MPI v2.5 Toolbox Diagnostic CLI Tool Request
 *                      message.
 *  07-26-12  02.00.10  Modified MPI2_TOOLBOX_DIAGNOSTIC_CLI_REQUEST so that
 *                      it uses MPI Chain SGE as well as MPI Simple SGE.
 *  08-19-13  02.00.11  Added MPI2_TOOLBOX_TEXT_DISPLAY_TOOL and related info.
 *  --------------------------------------------------------------------------
 */

#ifndef MPI2_TOOL_H
#define MPI2_TOOL_H

/*****************************************************************************
 *
 *               Toolbox Messages
 *
 *****************************************************************************/

/* defines for the Tools */
#define MPI2_TOOLBOX_CLEAN_TOOL                     (0x00)
#define MPI2_TOOLBOX_MEMORY_MOVE_TOOL               (0x01)
#define MPI2_TOOLBOX_DIAG_DATA_UPLOAD_TOOL          (0x02)
#define MPI2_TOOLBOX_ISTWI_READ_WRITE_TOOL          (0x03)
#define MPI2_TOOLBOX_BEACON_TOOL                    (0x05)
#define MPI2_TOOLBOX_DIAGNOSTIC_CLI_TOOL            (0x06)
#define MPI2_TOOLBOX_TEXT_DISPLAY_TOOL              (0x07)
```

```
 87 /*****************************************************************************
 88 *  Toolbox reply
 89 *****************************************************************************/

 91 typedef struct _MPI2_TOOLBOX_REPLY
 92 {
 93     U8                      Tool;                   /* 0x00 */
 94     U8                      Reserved1;              /* 0x01 */
 95     U8                      MsgLength;              /* 0x02 */
 96     U8                      Function;               /* 0x03 */
 97     U16                     Reserved2;              /* 0x04 */
 98     U8                      Reserved3;              /* 0x06 */
 99     U8                      MsgFlags;               /* 0x07 */
100     U8                      VP_ID;                  /* 0x08 */
101     U8                      VF_ID;                  /* 0x09 */
102     U16                     Reserved4;              /* 0x0A */
103     U16                     Reserved5;              /* 0x0C */
104     U16                     IOCStatus;              /* 0x0E */
105     U32                     IOCLogInfo;             /* 0x10 */
106 } MPI2_TOOLBOX_REPLY, MPI2_POINTER PTR_MPI2_TOOLBOX_REPLY,
______unchanged_portion_omitted_
161   Mpi2ToolboxMemMoveRequest_t, MPI2_POINTER pMpi2ToolboxMemMoveRequest_t;


164 /*****************************************************************************
165 *  Toolbox Diagnostic Data Upload request
166 *****************************************************************************/

168 typedef struct _MPI2_TOOLBOX_DIAG_DATA_UPLOAD_REQUEST
169 {
170     U8                      Tool;                   /* 0x00 */
171     U8                      Reserved1;              /* 0x01 */
172     U8                      ChainOffset;            /* 0x02 */
173     U8                      Function;               /* 0x03 */
174     U16                     Reserved2;              /* 0x04 */
175     U8                      Reserved3;              /* 0x06 */
176     U8                      MsgFlags;               /* 0x07 */
177     U8                      VP_ID;                  /* 0x08 */
178     U8                      VF_ID;                  /* 0x09 */
179     U16                     Reserved4;              /* 0x0A */
180     U8                      SGLFlags;               /* 0x0C */
181     U8                      Reserved5;              /* 0x0D */
182     U16                     Reserved6;              /* 0x0E */
183     U32                     Flags;                  /* 0x10 */
184     U32                     DataLength;             /* 0x14 */
185     MPI2_SGE_SIMPLE_UNION   SGL;                    /* 0x18 */
186 } MPI2_TOOLBOX_DIAG_DATA_UPLOAD_REQUEST,
187   MPI2_POINTER PTR_MPI2_TOOLBOX_DIAG_DATA_UPLOAD_REQUEST,
188   Mpi2ToolboxDiagDataUploadRequest_t,
189   MPI2_POINTER pMpi2ToolboxDiagDataUploadRequest_t;

191 /* use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */


194 typedef struct _MPI2_DIAG_DATA_UPLOAD_HEADER
195 {
196     U32                     DiagDataLength;         /* 00h */
197     U8                      FormatCode;             /* 04h */
198     U8                      Reserved1;              /* 05h */
199     U16                     Reserved2;              /* 06h */
200 } MPI2_DIAG_DATA_UPLOAD_HEADER, MPI2_POINTER PTR_MPI2_DIAG_DATA_UPLOAD_HEADER,
201   Mpi2DiagDataUploadHeader_t, MPI2_POINTER pMpi2DiagDataUploadHeader_t;
```



```
204 /*****************************************************************************
205 *  Toolbox ISTWI Read Write Tool
206 *****************************************************************************/

208 /* Toolbox ISTWI Read Write Tool request message */
209 typedef struct _MPI2_TOOLBOX_ISTWI_READ_WRITE_REQUEST
210 {
211     U8                      Tool;                   /* 0x00 */
212     U8                      Reserved1;              /* 0x01 */
213     U8                      ChainOffset;            /* 0x02 */
214     U8                      Function;               /* 0x03 */
215     U16                     Reserved2;              /* 0x04 */
216     U8                      Reserved3;              /* 0x06 */
217     U8                      MsgFlags;               /* 0x07 */
218     U8                      VP_ID;                  /* 0x08 */
219     U8                      VF_ID;                  /* 0x09 */
220     U16                     Reserved4;              /* 0x0A */
221     U32                     Reserved5;              /* 0x0C */
222     U32                     Reserved6;              /* 0x10 */
223     U8                      DevIndex;               /* 0x14 */
224     U8                      Action;                 /* 0x15 */
225     U8                      SGLFlags;               /* 0x16 */
226     U8                      Flags;                  /* 0x17 */
189     U8                      Reserved7;              /* 0x17 */
227     U16                     TxDataLength;           /* 0x18 */
228     U16                     RxDataLength;           /* 0x1A */
229     U32                     Reserved8;              /* 0x1C */
230     U32                     Reserved9;              /* 0x20 */
231     U32                     Reserved10;             /* 0x24 */
232     U32                     Reserved11;             /* 0x28 */
233     U32                     Reserved12;             /* 0x2C */
234     MPI2_SGE_SIMPLE_UNION   SGL;                    /* 0x30 */
235 } MPI2_TOOLBOX_ISTWI_READ_WRITE_REQUEST,
236   MPI2_POINTER PTR_MPI2_TOOLBOX_ISTWI_READ_WRITE_REQUEST,
237   Mpi2ToolboxIstwiReadWriteRequest_t,
238   MPI2_POINTER pMpi2ToolboxIstwiReadWriteRequest_t;

240 /* values for the Action field */
241 #define MPI2_TOOL_ISTWI_ACTION_READ_DATA            (0x01)
242 #define MPI2_TOOL_ISTWI_ACTION_WRITE_DATA           (0x02)
243 #define MPI2_TOOL_ISTWI_ACTION_SEQUENCE             (0x03)
244 #define MPI2_TOOL_ISTWI_ACTION_RESERVE_BUS          (0x10)
245 #define MPI2_TOOL_ISTWI_ACTION_RELEASE_BUS          (0x11)
246 #define MPI2_TOOL_ISTWI_ACTION_RESET                (0x12)

248 /* use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */
211 /* values for SGLFlags field are in the SGL section of mpi2.h */

250 /* values for the Flags field */
251 #define MPI2_TOOL_ISTWI_FLAG_AUTO_RESERVE_RELEASE   (0x80)
252 #define MPI2_TOOL_ISTWI_FLAG_PAGE_ADDR_MASK         (0x07)


255 /* Toolbox ISTWI Read Write Tool reply message */
256 typedef struct _MPI2_TOOLBOX_ISTWI_REPLY
257 {
258     U8                      Tool;                   /* 0x00 */
259     U8                      Reserved1;              /* 0x01 */
260     U8                      MsgLength;              /* 0x02 */
261     U8                      Function;               /* 0x03 */
262     U16                     Reserved2;              /* 0x04 */
263     U8                      Reserved3;              /* 0x06 */
264     U8                      MsgFlags;               /* 0x07 */
265     U8                      VP_ID;                  /* 0x08 */
266     U8                      VF_ID;                  /* 0x09 */
267     U16                     Reserved4;              /* 0x0A */
```

```
    U16                     Reserved5;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
    U8                      DevIndex;                   /* 0x14 */
    U8                      Action;                     /* 0x15 */
    U8                      IstwiStatus;                /* 0x16 */
    U8                      Reserved6;                  /* 0x17 */
    U16                     TxDataCount;                /* 0x18 */
    U16                     RxDataCount;                /* 0x1A */
} MPI2_TOOLBOX_ISTWI_REPLY, MPI2_POINTER PTR_MPI2_TOOLBOX_ISTWI_REPLY,
_____unchanged_portion_omitted_
  Mpi2ToolboxBeaconRequest_t, MPI2_POINTER pMpi2ToolboxBeaconRequest_t;

/* values for the Flags field */
#define MPI2_TOOLBOX_FLAGS_BEACONMODE_OFF       (0x00)
#define MPI2_TOOLBOX_FLAGS_BEACONMODE_ON        (0x01)


/*****************************************************************************
*  Toolbox Diagnostic CLI Tool
*****************************************************************************/

#define MPI2_TOOLBOX_DIAG_CLI_CMD_LENGTH    (0x5C)

/* MPI v2.0 Toolbox Diagnostic CLI Tool request message */
/* Toolbox Diagnostic CLI Tool request message */
typedef struct _MPI2_TOOLBOX_DIAGNOSTIC_CLI_REQUEST
{
    U8                      Tool;                       /* 0x00 */
    U8                      Reserved1;                  /* 0x01 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U8                      SGLFlags;                   /* 0x0C */
    U8                      Reserved5;                  /* 0x0D */
    U16                     Reserved6;                  /* 0x0E */
    U32                     DataLength;                 /* 0x10 */
    U8                      DiagnosticCliCommand[MPI2_TOOLBOX_DIAG_CLI_CMD_LENGT
    MPI2_MPI_SGE_IO_UNION   SGL;                        /* 0x70 */
    MPI2_SGE_SIMPLE_UNION   SGL;                        /* 0x70 */
} MPI2_TOOLBOX_DIAGNOSTIC_CLI_REQUEST,
  MPI2_POINTER PTR_MPI2_TOOLBOX_DIAGNOSTIC_CLI_REQUEST,
  Mpi2ToolboxDiagnosticCliRequest_t,
  MPI2_POINTER pMpi2ToolboxDiagnosticCliRequest_t;

/* use MPI2_SGLFLAGS_ defines from mpi2.h for the SGLFlags field */
/* values for SGLFlags field are in the SGL section of mpi2.h */


/* MPI v2.5 Toolbox Diagnostic CLI Tool request message */
typedef struct _MPI25_TOOLBOX_DIAGNOSTIC_CLI_REQUEST
{
    U8                      Tool;                       /* 0x00 */
    U8                      Reserved1;                  /* 0x01 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
```



```
    U16                     Reserved4;                  /* 0x0A */
    U32                     Reserved5;                  /* 0x0C */
    U32                     DataLength;                 /* 0x10 */
    U8                      DiagnosticCliCommand[MPI2_TOOLBOX_DIAG_CLI_CMD_LENGT
    MPI25_SGE_IO_UNION      SGL;                        /* 0x70 */
} MPI25_TOOLBOX_DIAGNOSTIC_CLI_REQUEST,
  MPI2_POINTER PTR_MPI25_TOOLBOX_DIAGNOSTIC_CLI_REQUEST,
  Mpi25ToolboxDiagnosticCliRequest_t,
  MPI2_POINTER pMpi25ToolboxDiagnosticCliRequest_t;


/* Toolbox Diagnostic CLI Tool reply message */
typedef struct _MPI2_TOOLBOX_DIAGNOSTIC_CLI_REPLY
{
    U8                      Tool;                       /* 0x00 */
    U8                      Reserved1;                  /* 0x01 */
    U8                      MsgLength;                  /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U16                     Reserved5;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
    U32                     ReturnedDataLength;         /* 0x14 */
} MPI2_TOOLBOX_DIAGNOSTIC_CLI_REPLY,
  MPI2_POINTER PTR_MPI2_TOOLBOX_DIAG_CLI_REPLY,
  Mpi2ToolboxDiagnosticCliReply_t,
  MPI2_POINTER pMpi2ToolboxDiagnosticCliReply_t;


/*****************************************************************************
*  Toolbox Console Text Display Tool
*****************************************************************************/

/* Toolbox Console Text Display Tool request message */
typedef struct _MPI2_TOOLBOX_TEXT_DISPLAY_REQUEST
{
    U8                      Tool;               /* 0x00 */
    U8                      Reserved1;          /* 0x01 */
    U8                      ChainOffset;        /* 0x02 */
    U8                      Function;           /* 0x03 */
    U16                     Reserved2;          /* 0x04 */
    U8                      Reserved3;          /* 0x06 */
    U8                      MsgFlags;           /* 0x07 */
    U8                      VP_ID;              /* 0x08 */
    U8                      VF_ID;              /* 0x09 */
    U16                     Reserved4;          /* 0x0A */
    U8                      Console;            /* 0x0C */
    U8                      Flags;              /* 0x0D */
    U16                     Reserved6;          /* 0x0E */
    U8                      TextToDisplay[4];   /* 0x10 */ /* actual length dete
} MPI2_TOOLBOX_TEXT_DISPLAY_REQUEST,
  MPI2_POINTER PTR_MPI2_TOOLBOX_TEXT_DISPLAY_REQUEST,
  Mpi2ToolboxTextDisplayRequest_t,
  MPI2_POINTER pMpi2ToolboxTextDisplayRequest_t;

/* defines for the Console field */
#define MPI2_TOOLBOX_CONSOLE_TYPE_MASK          (0xF0)
#define MPI2_TOOLBOX_CONSOLE_TYPE_DEFAULT       (0x00)
#define MPI2_TOOLBOX_CONSOLE_TYPE_UART          (0x10)
#define MPI2_TOOLBOX_CONSOLE_TYPE_ETHERNET      (0x20)
```

```
#define MPI2_TOOLBOX_CONSOLE_NUMBER_MASK        (0x0F)

/* defines for the Flags field */
#define MPI2_TOOLBOX_CONSOLE_FLAG_TIMESTAMP     (0x01)



/*****************************************************************************
*
*       Diagnostic Buffer Messages
*
*****************************************************************************/


/*****************************************************************************
*  Diagnostic Buffer Post request
*****************************************************************************/

typedef struct _MPI2_DIAG_BUFFER_POST_REQUEST
{
    U8                      ExtendedType;               /* 0x00 */
    U8                      BufferType;                 /* 0x01 */
    U8                      ChainOffset;                /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U64                     BufferAddress;              /* 0x0C */
    U32                     BufferLength;               /* 0x14 */
    U32                     Reserved5;                  /* 0x18 */
    U32                     Reserved6;                  /* 0x1C */
    U32                     Flags;                      /* 0x20 */
    U32                     ProductSpecific[23];        /* 0x24 */
} MPI2_DIAG_BUFFER_POST_REQUEST, MPI2_POINTER PTR_MPI2_DIAG_BUFFER_POST_REQUEST,
  Mpi2DiagBufferPostRequest_t, MPI2_POINTER pMpi2DiagBufferPostRequest_t;

/* values for the ExtendedType field */
#define MPI2_DIAG_EXTENDED_TYPE_UTILIZATION         (0x02)

/* values for the BufferType field */
#define MPI2_DIAG_BUF_TYPE_TRACE                    (0x00)
#define MPI2_DIAG_BUF_TYPE_SNAPSHOT                 (0x01)
#define MPI2_DIAG_BUF_TYPE_EXTENDED                 (0x02)
/* count of the number of buffer types */
#define MPI2_DIAG_BUF_TYPE_COUNT                    (0x03)

/* values for the Flags field */
#define MPI2_DIAG_BUF_FLAG_RELEASE_ON_FULL          (0x00000002) /* for MPI v2.0
#define MPI2_DIAG_BUF_FLAG_IMMEDIATE_RELEASE        (0x00000001)


/*****************************************************************************
*  Diagnostic Buffer Post reply
*****************************************************************************/

typedef struct _MPI2_DIAG_BUFFER_POST_REPLY
{
    U8                      ExtendedType;               /* 0x00 */
    U8                      BufferType;                 /* 0x01 */
    U8                      MsgLength;                  /* 0x02 */
    U8                      Function;                   /* 0x03 */
    U16                     Reserved2;                  /* 0x04 */
    U8                      Reserved3;                  /* 0x06 */
```



```
    U8                      MsgFlags;                   /* 0x07 */
    U8                      VP_ID;                      /* 0x08 */
    U8                      VF_ID;                      /* 0x09 */
    U16                     Reserved4;                  /* 0x0A */
    U16                     Reserved5;                  /* 0x0C */
    U16                     IOCStatus;                  /* 0x0E */
    U32                     IOCLogInfo;                 /* 0x10 */
    U32                     TransferLength;             /* 0x14 */
} MPI2_DIAG_BUFFER_POST_REPLY, MPI2_POINTER PTR_MPI2_DIAG_BUFFER_POST_REPLY,
_____unchanged_portion_omitted_
```

```
**********************************************************
    3757 Tue Jun 17 10:46:19 2014
new/usr/src/uts/common/sys/scsi/adapters/mpt_sas/mpi/mpi2_type.h
NEX-1888 upstream
**********************************************************
```

```
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 */

/*
 *          Name:  mpi2_type.h
 *         Title:  MPI basic type definitions
 *  Creation Date:  August 16, 2006
 *
 *    mpi2_type.h Version:  02.00.00
 *
 *  Version History
 *  ---------------
 *
 *  Date      Version   Description
 *  --------  --------  ------------------------------------------------------
 *  04-30-07  02.00.00  Corresponds to Fusion-MPT MPI Specification Rev A.
 *  ------------------------------------------------------------------------
 */

#ifndef MPI2_TYPE_H
#define MPI2_TYPE_H


/*****************************************************************************
 * Define MPI2_POINTER if it hasn't already been defined. By default
 * MPI2_POINTER is defined to be a near pointer. MPI2_POINTER can be defined as
 * a far pointer by defining MPI2_POINTER as "far *" before this header file is
 * included.
 */
#ifndef MPI2_POINTER
#define MPI2_POINTER     *
#endif

/* the basic types may have already been included by mpi_type.h */
#ifndef MPI_TYPE_H
/*****************************************************************************
*
*               Basic Types
*
*****************************************************************************/

typedef signed   char   S8;
typedef unsigned char   U8;
typedef signed   short  S16;
typedef unsigned short  U16;

#ifdef  __FreeBSD__

typedef int32_t  S32;
typedef uint32_t U32;

#else

#if defined(unix) || defined(__arm) || defined(ALPHA) || defined(__PPC__) || def

    typedef signed   int   S32;
```

```
  86     typedef unsigned int   U32;

  88 #else

  90     typedef signed   long  S32;
  91     typedef unsigned long  U32;

  93 #endif
  94 #endif


  96 typedef struct _S64
  97 {
  98     U32          Low;
  99     S32          High;
 100 } S64;
```

*unchanged_portion_omitted_*